ELECTRONIC CIRCUITS
&
PULSE CIRCUITS

LABORATORY MANUAL

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGG

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY
(Sponsored by CMR Educational Society)
(Affiliated to JNTU, Hyderabad)
Secunderabad-14.

ELECTRONICS & COMMUNICATION ENGINEERING

VISION

To evolve into a center of excellence in Engineering Technology through creative and innovative practices in teaching-learning, promoting academic achievement & research excellence to produce internationally accepted competitive and world class professionals.

MISSION

To provide high quality academic programmes, training activities, research facilities and opportunities supported by continuous industry institute interaction aimed at employability, entrepreneurship, leadership and research aptitude among students.

QUALITY POLICY

- **Impart up-to-date knowledge to the students in Electronics & Communication area to make them quality engineers.**
- **Make the students experience the applications on quality equipment and tools.**
- **Provide systems, resources and training opportunities to achieve continuous improvement.**
- **Maintain global standards in education, training and services.**

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO1: PROFESSIONALISM & CITIZENSHIP

To create and sustain a community of learning in which students acquire knowledge and learn to apply it professionally with due consideration for ethical, ecological and economic issues.

PEO2: TECHNICAL ACCOMPLISHMENTS

To provide knowledge based services to satisfy the needs of society and the industry by providing hands on experience in various technologies in core field.

PEO3: INVENTION, INNOVATION AND CREATIVITY

To make the students to design, experiment, analyze, interpret in the core field with the help of other multi disciplinary concepts wherever applicable.

PEO4: PROFESSIONAL DEVELOPMENT

To educate the students to disseminate research findings with good soft skills and become a successful entrepreneur.

PEO5: HUMAN RESOURCE DEVELOPMENT

To graduate the students in building national capabilities in technology, education and research.

PROGRAMME SPECIFIC OBJECTIVES (PSOs)

PSO1

To develop a student community who acquire knowledge by ethical learning and fulfill the societal and industry needs in various technologies of core field.

PSO2

To nurture the students in designing, analyzing and interpreting required in research and development with exposure in multi disciplinary technologies in order to mould them as successful industry ready engineers/entrepreneurs

PSO3

To empower students with all round capabilities who will be useful in making nation strong in technology, education and research domains.

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design / development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multi disciplinary environments.
12. **Life- long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

LIST OF EXPERIMENTS

PART-I: ELECTRONIC CIRCUITS

CYCLE-I: SIMULATION USING MULTISIM

CYCLE-II: HARDWARE EXPERIMENTS

PART-II: PULSE CIRCUITS

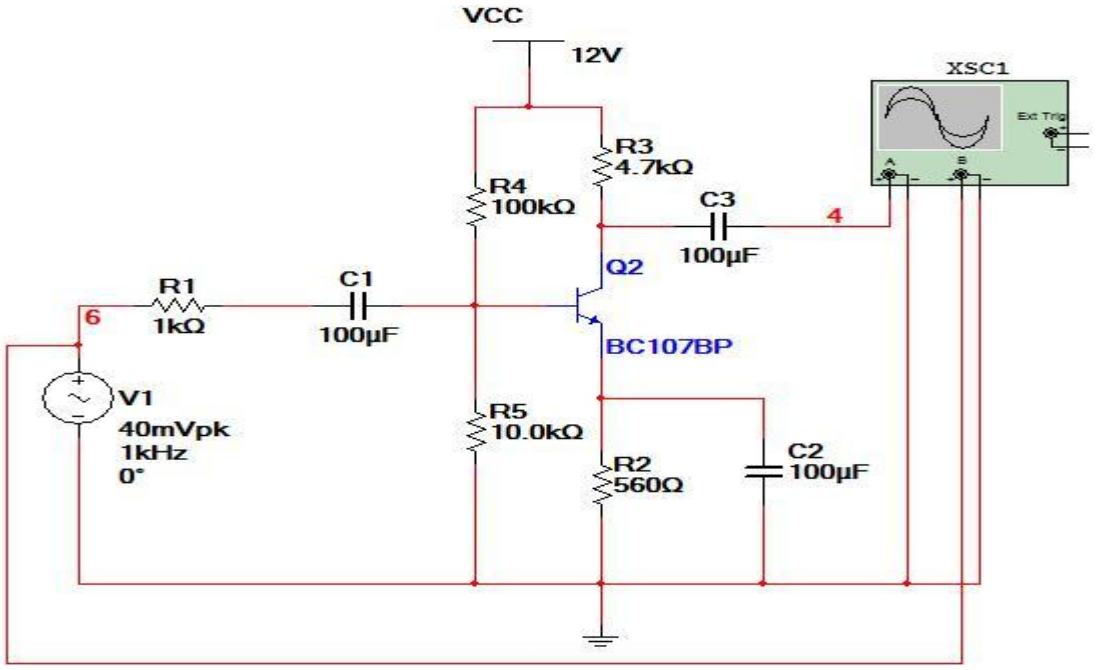
EXPERIMENT NO: 1
COMMON EMITTER AMPLIFIER

AIM:

To determine the gain and bandwidth of a CE Amplifier from its frequency response curve.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:

The single stage common emitter amplifier circuit shown above uses what is commonly called "Voltage Divider Biasing" or “self biasing”. This type of biasing arrangement uses two resistors as a potential divider network and is commonly used in the design of bipolar transistor amplifier circuits. This type of biasing arrangement greatly reduces the effects of varying Beta, (β) by holding the Base bias at a constant steady voltage. This type of biasing produces the greatest stability.

The Common Emitter Amplifier circuit has a resistor in its Collector circuit. The current flowing through this resistor produces the voltage output of the amplifier. The value of this resistor is chosen so that at the amplifiers quiescent operating point, Q-point this output voltage lies half way along the transistors load line. In Common Emitter Amplifier circuits, capacitors C1 and C2 are used as Coupling Capacitors to separate the AC signals from the DC biasing voltage. This ensures that the bias condition set up for the circuit to operate correctly is not effected by any additional amplifier stages, as the capacitors will only pass AC signals and block any DC component.

The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, C_E is included in the Emitter leg circuit. This capacitor is an open circuit component for DC bias meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor short circuits the Emitter resistor at high frequency signals and only R_L plus a very small internal resistance acts as the transistors load increasing the voltage gain to its maximum.

Generally, the value of the bypass capacitor, C_E is chosen to provide a reactance of at most, 1/10th the value of R_E at the lowest operating signal frequency. A single stage Common Emitter Amplifier is also an "Inverting Amplifier" as an increase in Base voltage causes a decrease in V out and a decrease in Base voltage produces an increase in Vout. The output signal is 180◦ out of phase with the input signal.

PROCEDURE:

1. Open the multisim icon in the system.

2. Place all the necessary components required for the design of the CE amplifier circuit i.e Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window.

3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.

4. Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.

5. Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.

6. To observe the frequency response, go to simulate-----► analysis-----►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.

7. A window opens showing the frequency response on the top and phase response at the bottom.

8. From the frequency response, calculate the bandwidth of the Amplifier.

9. To obtain the netlist, go to transfer-----►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

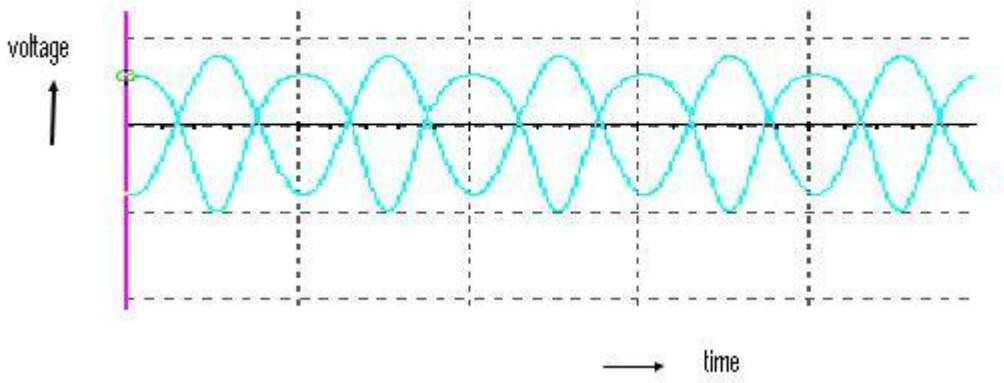
OBSERVATION TABLE:

S.NO	FREQUENCY(Hz)	GAIN(dB)

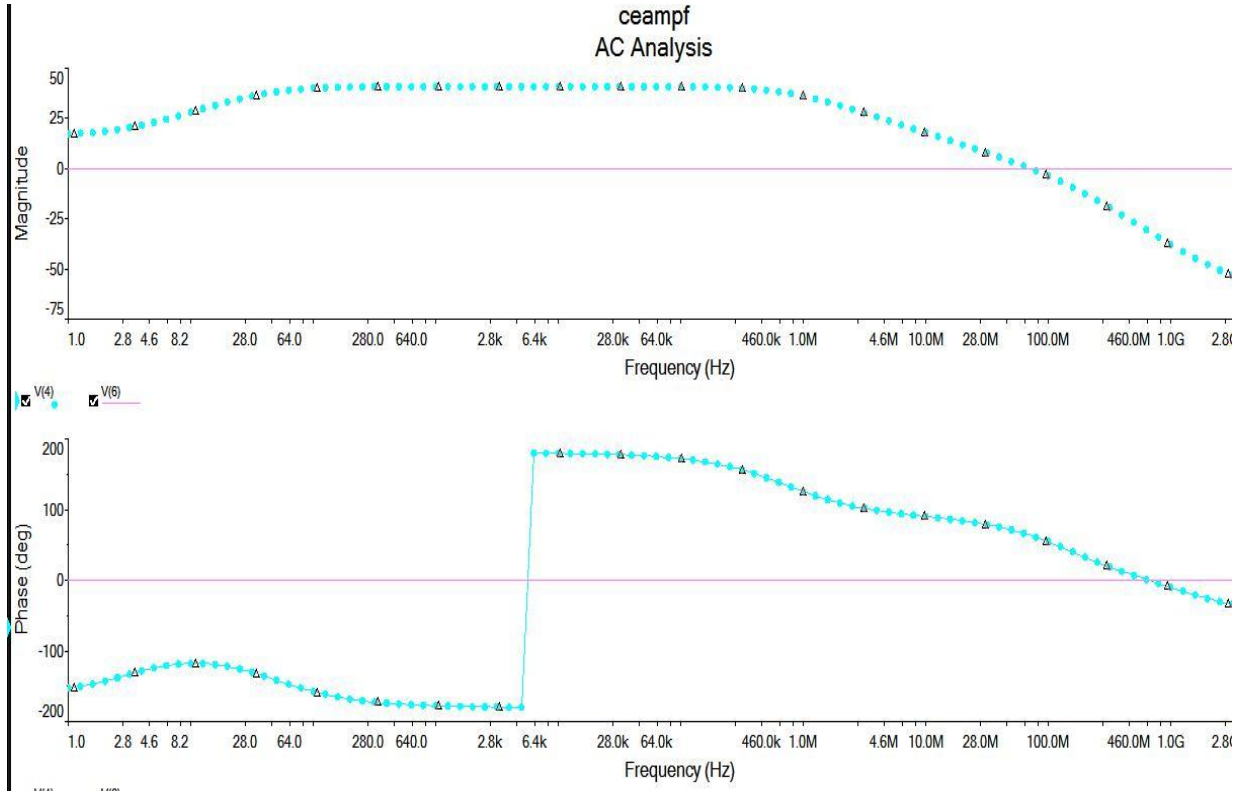
Bandwidth of the CE amplifier = f_h-f_l HZ

EXPECTED GRAPH:

INPUT VS OUTPUT WAVEFORMS



FREQUENCY RESPONSE AND PHASE RESPONSE GRAPHS



RESULT:
The maximum gain is _____dB and bandwidth is _____Hz of the CE Amplifier.

QUESTIONS:

1. What is the phase difference between input and output waveforms of CE amplifier?
2. What type of biasing is used in the given circuit?
3. If the given transistor is replaced by P-N-P, can we get the output or not?
4. What is the effect of emitter bypass capacitor on frequency response?
5. What is the effect of coupling capacitor?
6. What is the region of transistor so that it operates as an amplifier?
7. Draw the h-parameter model of CE amplifier.
8. How does transistor acts as an amplifier.
9. Mention the characteristics of CE amplifier.

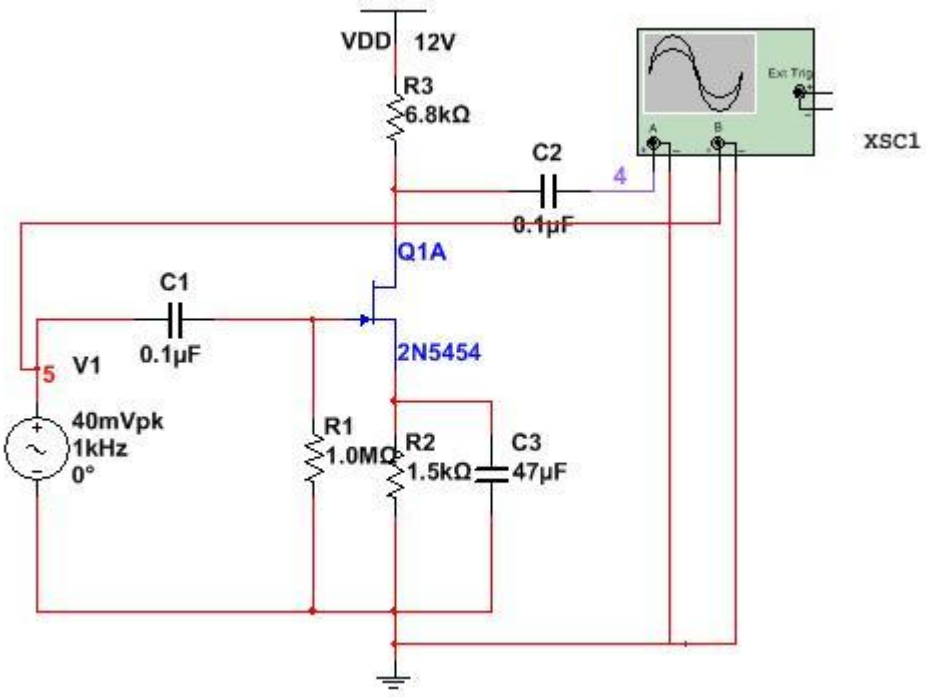
EXPERIMENT NO: 2
COMMON SOURCE AMPLIFIER

AIM:

To determine the Bandwidth from the frequency response of the Common Source FET Amplifier.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide- semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes.

In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P -N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle.

The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes. A common source amplifier FET amplifier has high input impedance and a moderate voltage gain. Also, the input and output voltages are 180 degrees out of Phase.

PROCEDURE:

1. Open the multisim icon in the system.

2. Place all the necessary components required for the design of the CS FET amplifier circuit i.e Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window.

3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.

3. Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.

4. Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.

5. To observe the frequency response, go to simulate-----► analysis-----►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.

6. A window opens showing the frequency response on the top and phase response at the bottom.

7. From the frequency response, calculate the bandwidth of the Amplifier.

8. To obtain the netlist, go to transfer-----►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit containing the specifications of all the used components used in the design of the circuit.

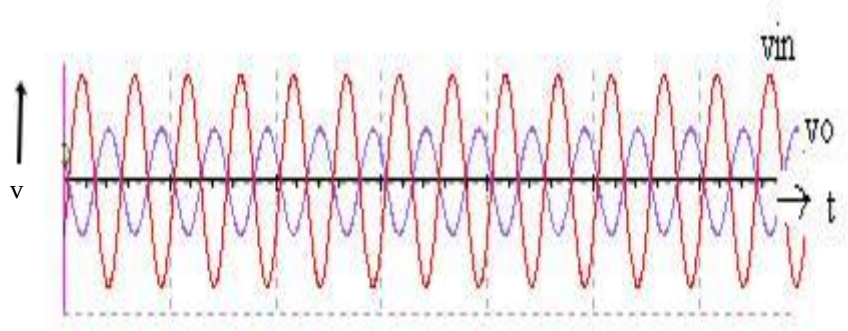
OBSERVATION TABLE:

S.NO	FREQUENCY(Hz)	GAIN(dB)

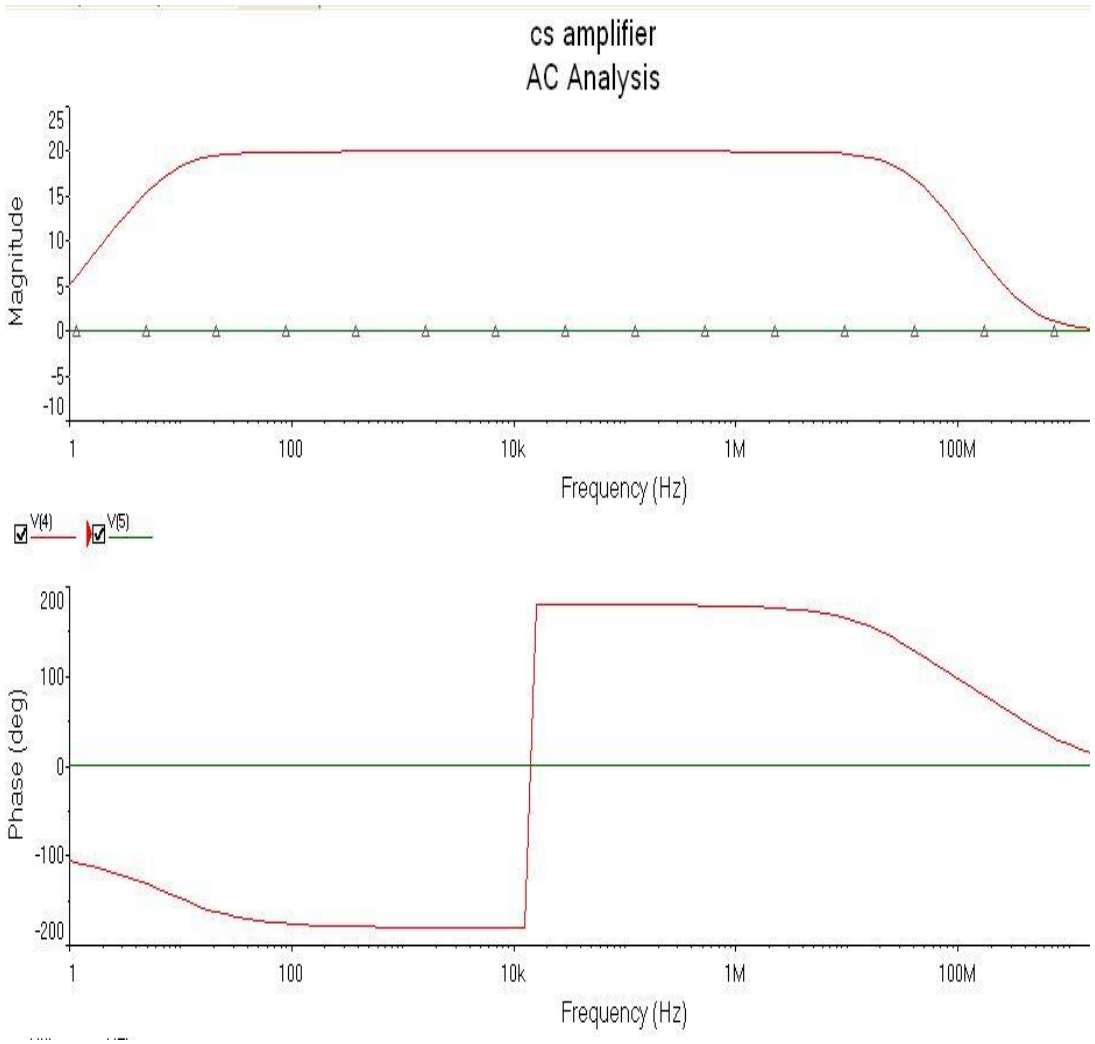
Bandwidth of the CE-CB Cascode amplifier=f_h-f_l Hz

MODEL GRAPH:

Input vs Output Waveforms



FREQUENCY RESPONSE:



RESULT: We have obtained the frequency response of the common Source FET Amplifier and also found its Bandwidth to be _____Hz.

QUESTIONS:

1. How does FET acts as an amplifier?
2. What are the parameters of a FET?
3. What is an amplification factor?
4. Draw the h-parameter model of the FET.
5. What are the advantages of FET over BJT?
6. What is the region of FET so that it acts as an amplifier?
7. What are the differences between JFET and MOSFET?
8. What type of biasing is used in the given circuit?

EXPERIMENT NO-3

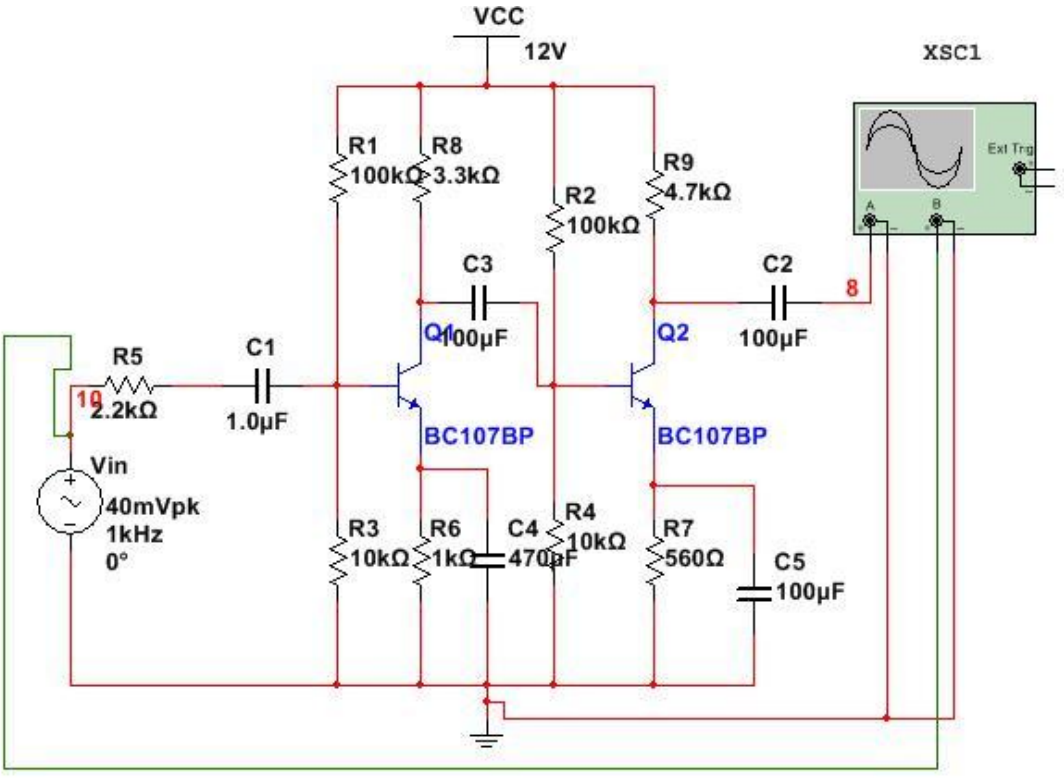
TWO STAGE RC-COUPLED AMPLIFIER

AIM:

To study the response of a two stage RC-coupled amplifier and calculate gain and band width.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:

As the gain provided by a single stage amplifier is usually not sufficient to drive the load, so to achieve extra gain multi-stage amplifier are used. In multi-stage amplifiers output of one-stage is coupled to the input of the next stage. The coupling of one stage to another is done with the help of some coupling devices. If it is coupled by RC then the amplifier is called RC -coupled amplifier. Frequency response of an amplifier is defined as the variation of gain with respective frequency. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at lower cut-off frequency and remains constant till higher cut-off frequency and then it falls again as the frequency increases. At low frequencies the reactance of coupling capacitor C_C is quite high and hence very small part of signal will pass through from one stage to the next stage.

At high frequencies the reactance of inter electrode capacitance is very small and behaves as a short circuit. This increases the loading effect on next stage and service to reduce the voltage gain due to these reasons the voltage gain drops at high frequencies.

At mid frequencies the effect of coupling capacitors is negligible and acts like short circuit, where as inter electrode capacitors acts like open circuit. So, the circuit becomes resistive at mid frequencies and the voltage gain remains constant during this range.

APPLICATIONS:

1. Audio amplifiers
2. Radio Transmitters and Receivers.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the two stage RC Coupled amplifier circuit i.e Resistors, Capacitors, Transistors,Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
4. Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.
5. Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.
6. To observe the frequency response, go to simulate-----► analysis-----►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.
7. A window opens showing the frequency response on the top and phase response at the bottom.
8. From the frequency response, calculate the bandwidth of the Amplifier.
9. To obtain the netlist, go to transfer-----►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

OBSERVATION TABLE:

S.NO	FREQUENCY(Hz)	GAIN(dB)

Bandwidth of the CE-CB Cascode amplifier=f_h-f_l Hz

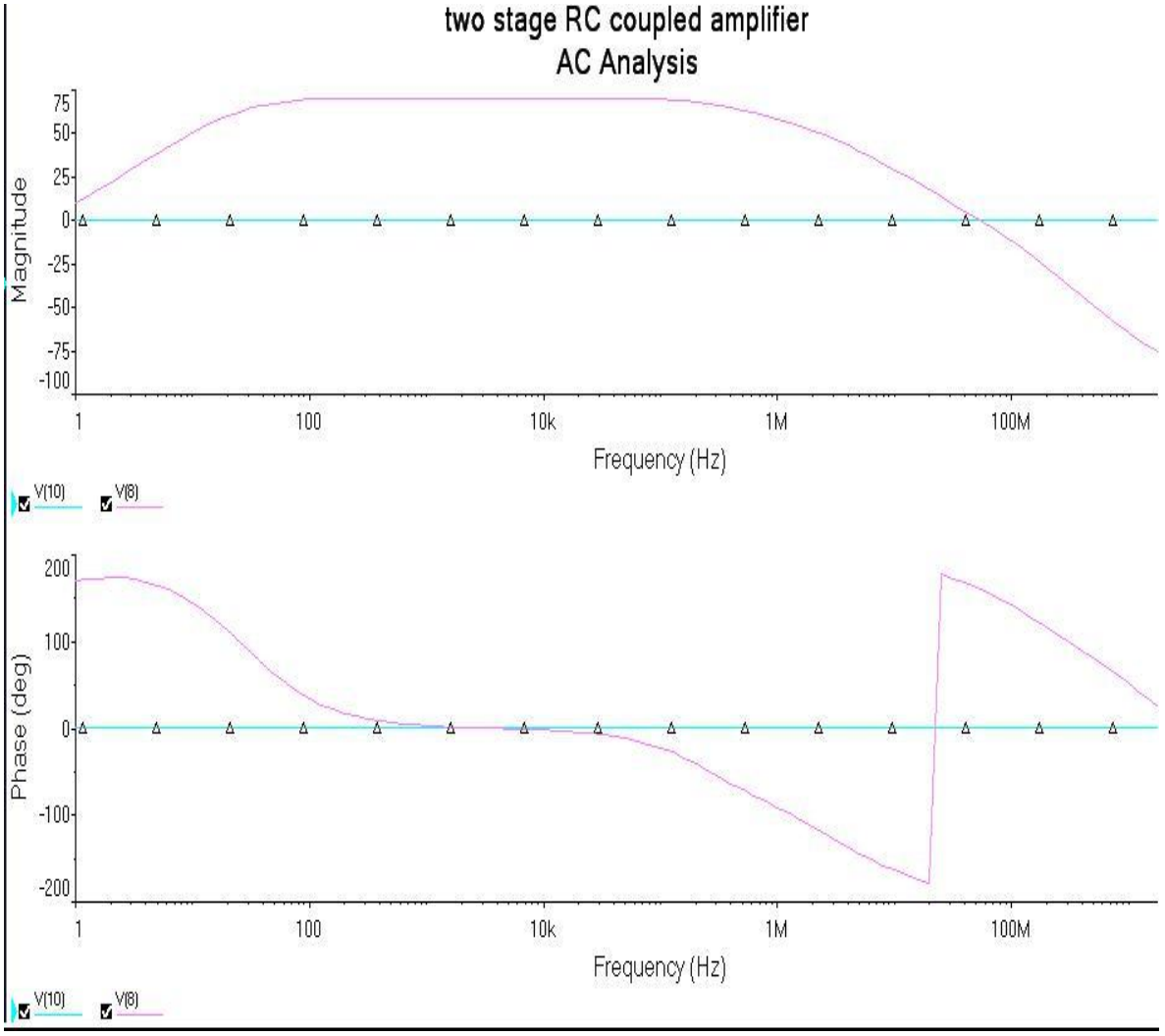
CALCULATIONS:

i. Determine lower cut-off frequency and upper cut-off frequency from the graph.

ii. Calculate Band width.

EXPECTED GRAPH:

Frequency Response:



RESULT:

The maximum gain is _____dB and bandwidth is _____Hz of the CE Amplifier.

QUESTIONS:

1. What are the advantages and disadvantages of multi-stage amplifiers?
2. Why gain falls at HF and LF?
3. Why the gain remains constant at MF?
4. Explain the function of emitter bypass capacitor, Ce?
5. How the band width will be effected as more number of stages are cascaded?
6. Define frequency response?
7. Give the formula for effective lower cut-off frequency, when N-number of stages are cascaded.
8. Explain the effect of coupling capacitors and inter-electrode capacitances on overall gain.
9. By how many times effective upper cut-off frequency will be reduced, if three identical stages are cascaded?
10. Mention the applications of two-stage RC-coupled amplifiers.

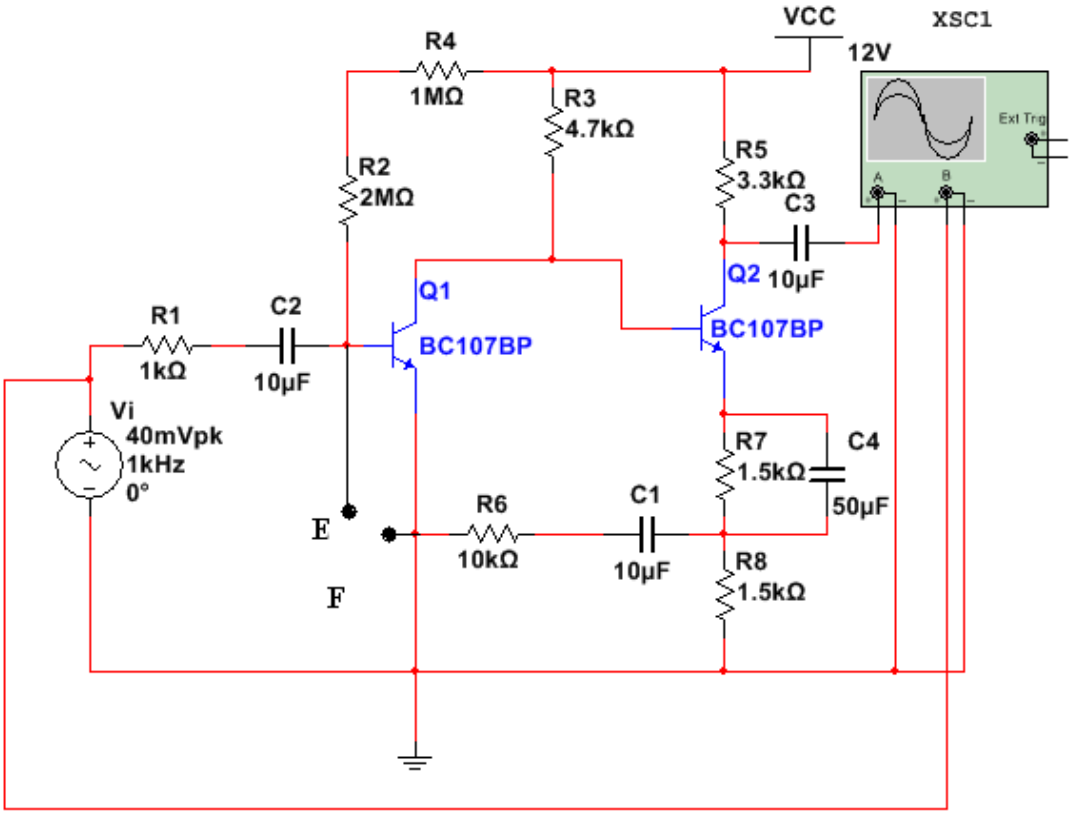
EXPERIMENT NO-4

CURRENT SHUNT FEEDBACK AMPLIFIER

AIM: To determine the effect of feedback on the frequency response of a current shunt feedback amplifier.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



PROCEDURE:

TO DETERMINE THE FREQUENCY RESPONSE WITH FEEDBACK

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the current shunt feedback amplifier circuit i.e Resistors, Capacitors, Diodes, Transistors, Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
3. Connect the channel of the Oscilloscope to the output of the circuit and by using the simulation switch and check output waveform.
4. To obtain the netlist, go to transfer-----►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

5. Vary the input frequency from 10Hz to 1MHz with input voltage constant (40mvpp) and note down the output voltage.

6. Calculate the voltage gain in dB using the formula Av=20 log(Vo/Vi).

TO DETERMINE THE FREQUENCY RESPONSE WITH FEEDBACK

1. Now connect E-F terminals in the circuit.

2. Connect the output of the feedback amplifier to the other channel of the CRO.

3. Vary the input frequency from 10Hz to 1MHz with input voltage constant (40mvpp) and note down the output voltage.

8. Calculate the voltage gain in dB using the formula Av=20 log (Vo/Vi).

OBSERVATIONS:

1. **WITHOUT FEEDBACK**

Vi= 40mvp-p at 1kHz

S.NO	FREQUENCY(Hz)	OUTPUT VOLTAGE (Vo)	VOLTAGE GAIN (Av=Vo/Vi)	GAIN (dB) Av=20 log (Vo/Vi).

Bandwidth without feedback=----------

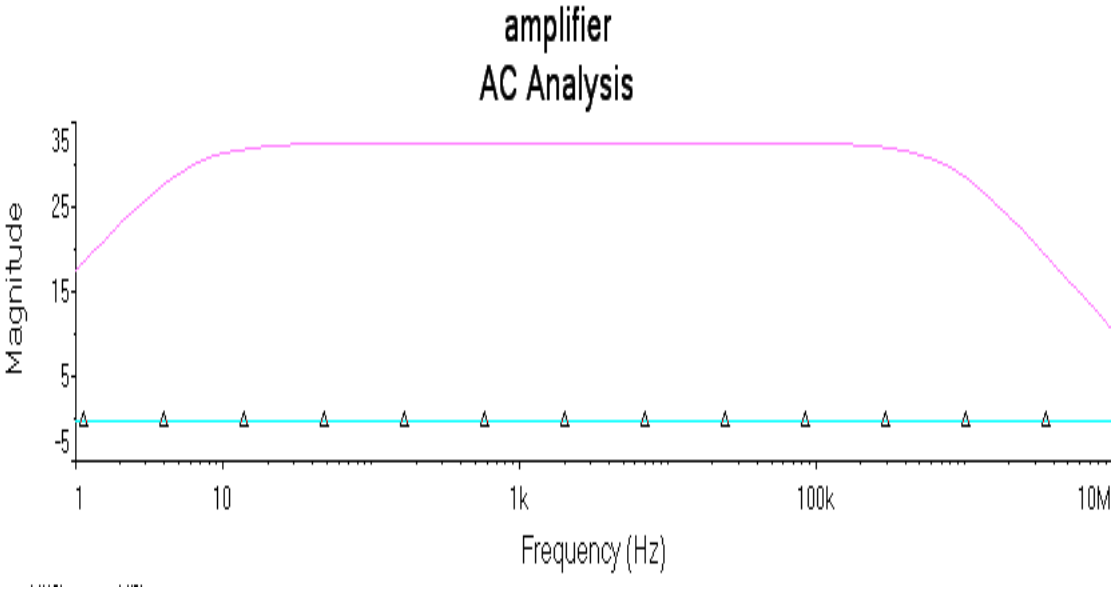
2. WITH FEEDBACK

Vi= 40mvp-p at 1kHz

S.NO	FREQUENCY(Hz)	OUTPUT VOLTAGE (Vo)	VOLTAGE GAIN (Avf=Vo/Vi)	GAIN (dB) Avf=20 log (Vo/Vi).

Bandwidth with feedback = ----------

EXPECTED GRAPH:



RESULT:

The Av of the current shunt feedback amplifier is ___ and the bandwidth is _____ without feedback and The Av of the current shunt feedback amplifier is ___ and the bandwidth is _____ with feedback.

QUESTIONS:

1. What is feedback?
2. What are the characteristics of feedback?
3. What is meant by sampling and mixing?
4. What are the configurations of feedback amplifiers?
5. What is the effect of feedback on an amplifier?
6. What is the effect of feedback on input and output resistances?

EXPERIMENT NO:5

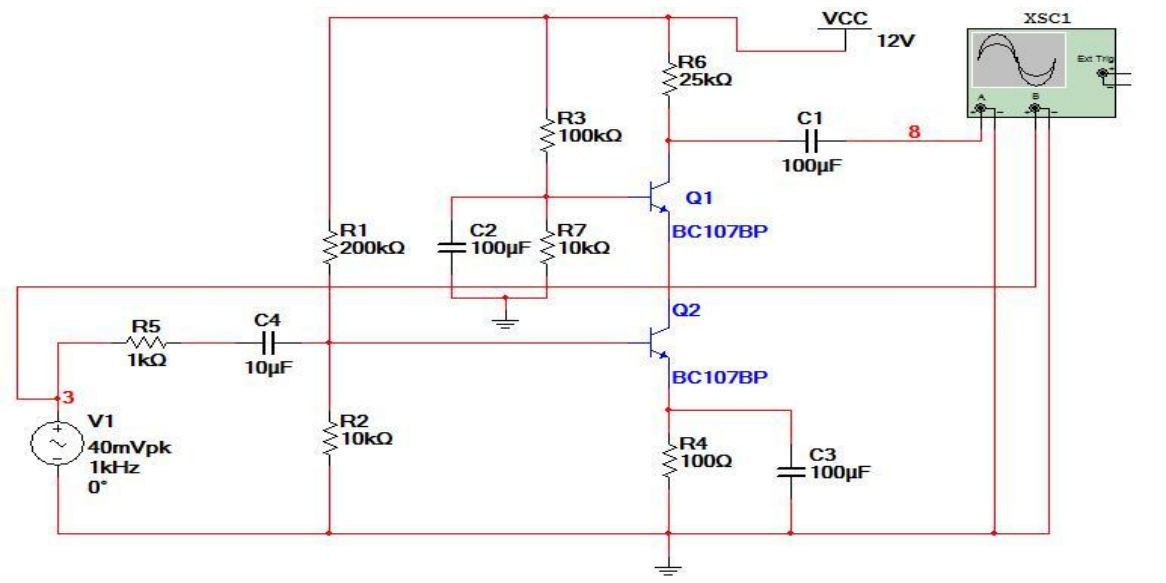
CE-CB CASCODE AMPLIFIER

AIM:

To determine the gain and bandwidth of a CE –CB Cascode Amplifier from its frequency response curve.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:



THEORY:

A Cascode amplifier consists of a common-emitter stage loaded by the emitter of a common-base stage. While the C-B (common-base) amplifier is known for wider bandwidth than the C-E (common-emitter) configuration, the low input impedance (10s of Ω) of C-B is a limitation for many applications. The solution is to precede the C-B stage by a low gain C-E stage which has moderately high input impedance (kΩs). The stages are in a cascode configuration, stacked in series, as opposed to cascaded for a standard amplifier chain. The cascode amplifier configuration has both wide bandwidth and moderately high input impedance. Before the invention of the RF dual gate MOSFET, the BJT Cascode amplifier could have been found in UHF (ultra high frequency) TV tuners. A Cascode amplifier has a high gain, moderately high input impedance, high output impedance, and a high bandwidth.

PROCEDURE:

1 Open the multisim icon in the system.

2 Place all the necessary components required for the design of the CE -CB cascode amplifier circuit i.e Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window.

3 Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.

4 Connect the two channels of the Oscilloscope to input and output of the circuit and by using the simulation switch and check the input and output waveforms.

5 Assign net numbers to input and output wires by double clicking on the particular wire and clicking on the show option.

6 To observe the frequency response, go to simulate-----► analysis-----►ac analysis and select the start and stop frequencies, select vertical scale as decibels, specify the output variables and click on simulate.

7 A window opens showing the frequency response on the top and phase response at the bottom.

8 From the frequency response, calculate the bandwidth of the Amplifier.

9 To obtain the net list, go to transfer-----►export netlist and save the net list in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

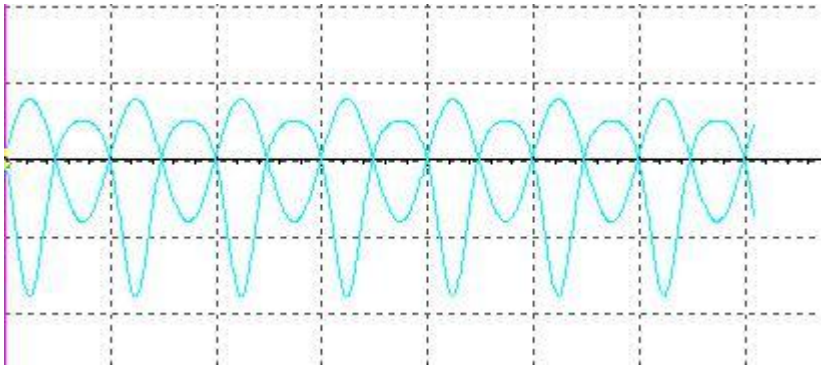
OBSERVATION TABLE:

S.NO	FREQUENCY(Hz)	GAIN(dB)

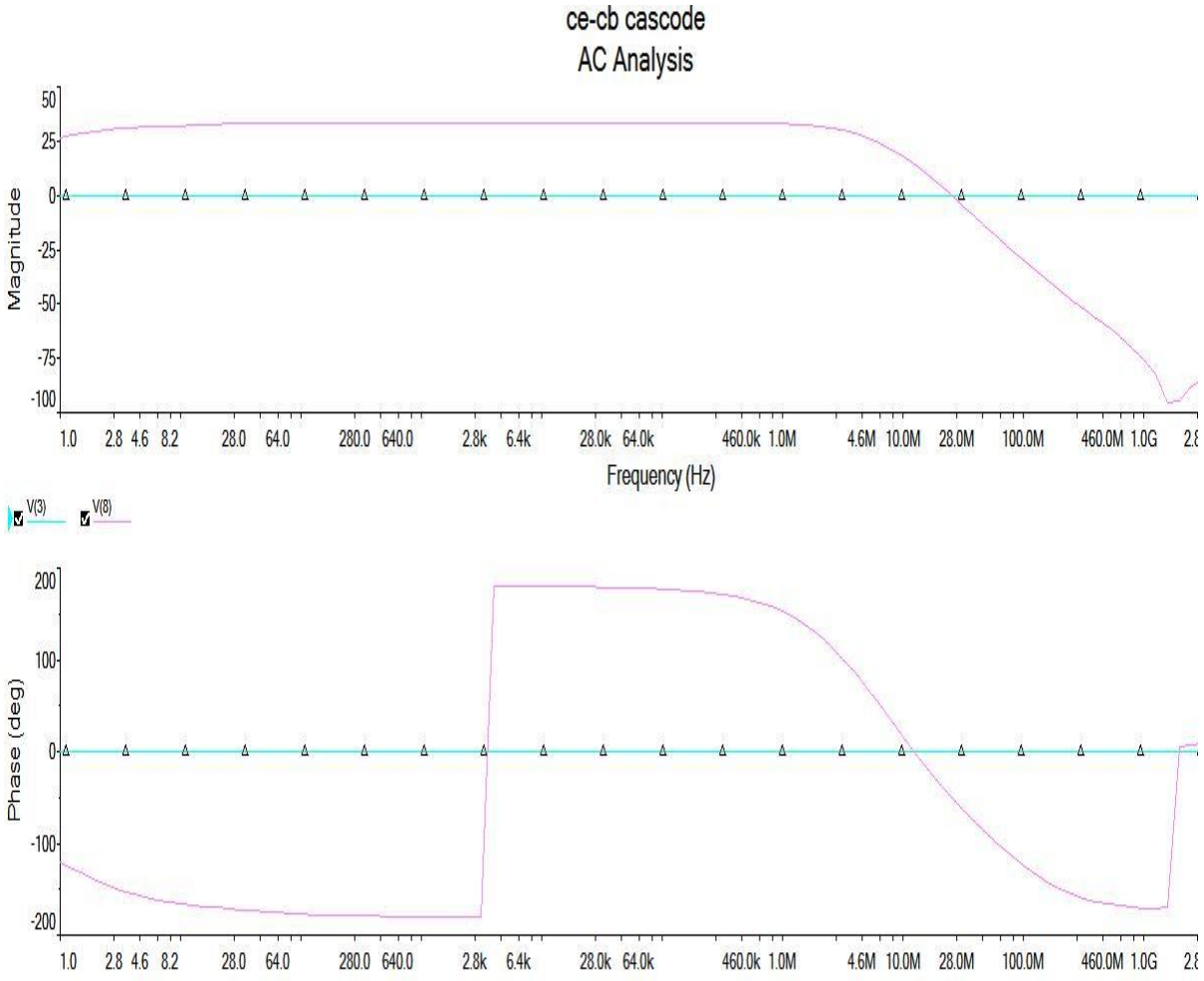
Bandwidth of the CE-CB Cascode amplifier=f_h-f_l Hz

EXPECTED GRAPH:

Input Vs Output waveforms



FREQUENCY RESPONSE AND PHASE RESPONSE GRAPHS



RESULT:

The maximum gain is _____dB and bandwidth is _____Hz of the CE - CB Cascode Amplifier**.**

QUESTIONS:

1. What is the difference between cascading and cascading?
2. What are the advantages of cascading?
3. What is the upper and lower cutoff frequencies of an n-stage cascaded amplifier?
4. What is the effective bandwidth of an n-stage Cascaded amplifier?
5. What is the preferred amplifier configuration for input stage in a cascade amplifier?
6. What is the preferred amplifier configuration for output stage in a cascade amplifier?
7. What is the preferred amplifier configuration for intermediate stage in a cascade amplifier?

EXPERIMENT NO-6

RC PHASESHIFT OSCILLATOR

AIM:

To determine the frequency of oscillation of an RC Phase Shift Oscillator.

SOFTWARE REQUIRED: Multisim

DESIGN PROCEDURE:

a) **Let R = 10K**

$$f_r = \frac{1}{2\pi R_C \sqrt{6+4K/10K}} \quad \text{When } K = \frac{R_C}{R}$$

$$C = \frac{1}{2\pi \times 10K \times 6K \sqrt{6+4\frac{4K}{10K}}}$$

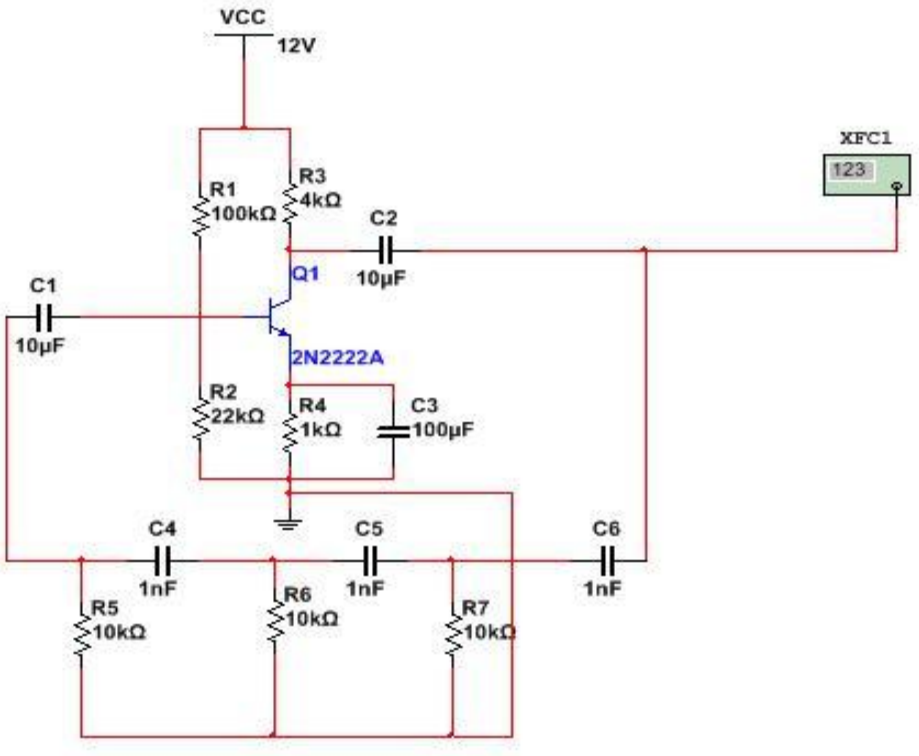
$= 0.962nF \approx 1nF$ (*Select s* tan *dard*)

$R = 10K$; $C = 1nF$

b) $hfe = 23 + \frac{29}{K} + 4K$ *for sustained oscillation*

≈ 97.1

CIRCUIT DIAGRAM:



PROCEDURE:

1 Open the multisim icon in the system.

2 Place all the necessary components required for the design of the RC Phase Shift Oscillator circuit i.e Resistors, Capacitors, Transistors, Voltage sources, Power sources, Ground etc on the design window.

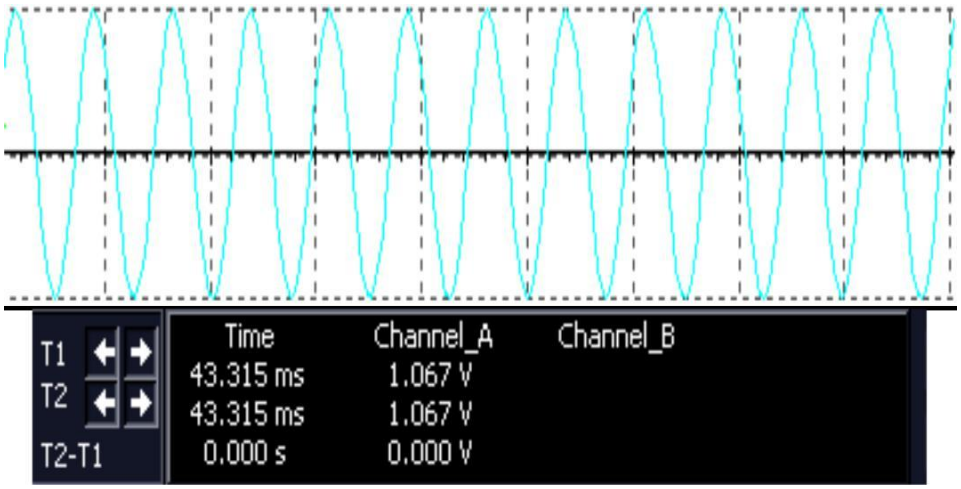
3 Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.

4 Connect a frequency counter and click on the simulate button.

5 The frequency of oscillation will be displayed on the simulation window.

6 To obtain the netlist, go to transfer-----►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

EXPECTED WAVEFORM:



RESULT: The frequency of oscillation of the RC Phase Shift Oscillator is _____Hz.

QUESTIONS:

1. What is an Oscillator circuit?
2. What is the main difference between an amplifier and an oscillator?
3. State Barkhausen criterion for oscillation.
4. State the factors on which oscillators can be classified.
5. Give the expression for the frequency of oscillation and the minimum gain required for sustained oscillations of the RC phase shift oscillator.
6. Why three RC networks are needed for a phase shift oscillator? Can it be two or four?
7. What are the merits and demerits of phase shift oscillator?
8. At low frequency which oscillators are found to be more suitable?
9. What are the two important RC oscillators?

EXPERIMENT NO-7

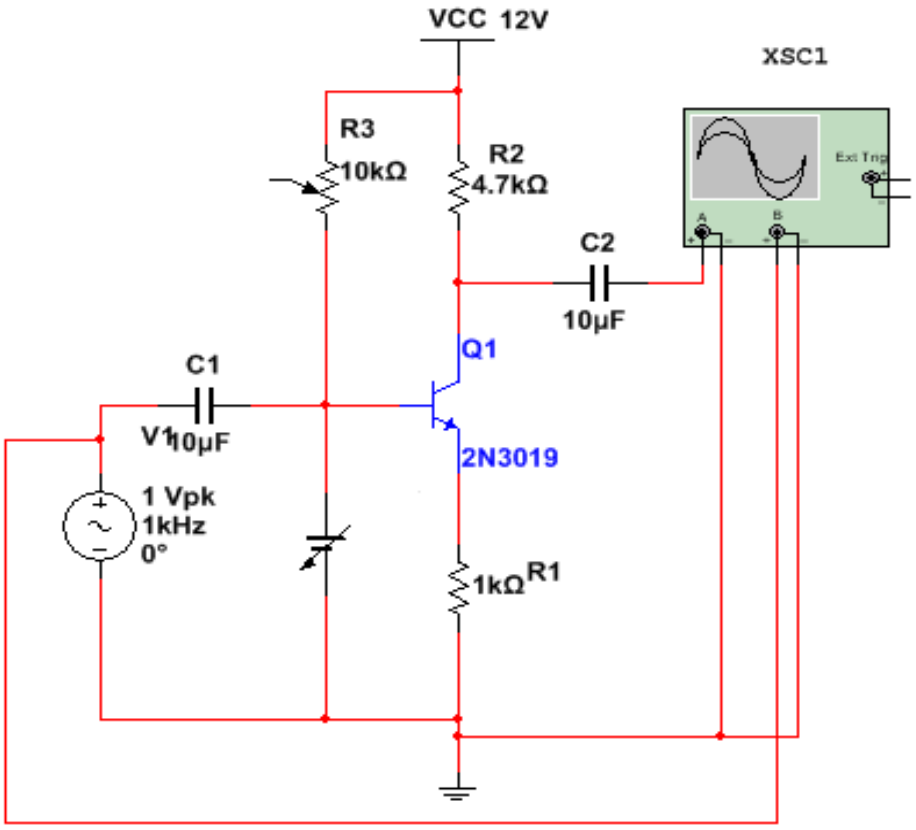
CLASS-A POWER AMPLIFIER

AIM:

To design a series fed class-A power amplifier in order to achieve max output ac power and efficiency.

EQUIPMENT REQUIRED: MULTISIM

CIRCUIT DIAGRAM:



THEORY:

The above circuit is called as "series fed" because the load R_L is connected in series with transistor output. It is also called as direct coupled amplifier.

I_{CQ} = Zero signal collector current

V_{CEQ} = Zero signal collector to emitter voltage

Power amplifiers are mainly used to deliver more power to the load. To deliver more power it requires large input signals, so generally power amplifiers are preceded by a series of voltage amplifiers. In class-A power amplifiers, Q-point is located in the middle of DC-load line. So output current flows for complete cycle of input signal. Under zero signal condition, maximum power dissipation occurs across the transistor. As the input signal amplitude increases power dissipation reduces The maximum theoretical efficiency is 25%.

APPLICATIONS:

This is used for low power linear applications in audio and wideband RF range, where high efficiency is not required.

EXTENSIONS:

In series fed class-A power amplifier we have calculated the efficiency i.e. how efficiently DC-power is converted into AC-power depending on the magnitude of input signal. Once we design a power amplifier for a particular efficiency, the circuit will not give that efficiency to all its input signals of different amplitudes. Hence, depending on the input signal we have to choose Vcc to obtain a particular efficiency. By employing Transformer coupling, efficiency can be improved to 50%.The experiment is conducted using low power transistors like BC107, SL100 only to get familiarity in biasing and measurement. Actual power amplifiers operate at 1 watt to 100 watts. This will call for operating transistors high current and small value resistors of greater than 1/4 to 1 watt which are used in the laboratory. Actual power amplifiers use heat sinks on the transistors.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the Complementary symmetry Class B Power amplifier circuit i.e Resistors,Capacitors, Diodes, Transistors, Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
4. Connect the channel of the Oscilloscope to the output of the circuit and by using the simulation switch and check output waveform.
5. To obtain the netlist, go to transfer-----►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

OBSERVATIONS:

Efficiency is defined as the ratio of AC output power to DC input power

DC input power = Vcc x I_{CQ}

AC output power = $V_{P\text{-}P}^2 / 8R_L$

CALCULATIONS:

Under zero signal condition:

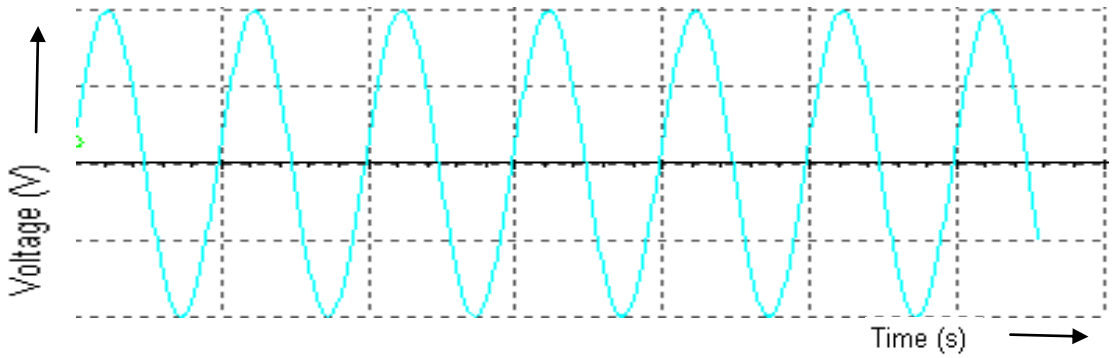
$Vcc = I_B R_B + V_{BE}$

$I_{BQ} = (Vcc - V_{BE}) / R_B$
$I_{CQ} = \beta \times I_{BQ}$

$V_{CE} = Vcc - I_C R_C$

EXPECTED GRAPH:

Vin=1V_{p-p}



RESULT:

1. The maximum input signal amplitude which produces undistorted output signal is _____
2. The practical efficiency of the circuit is _____
3. The efficiency observed is _____ against theoretical maximum of 25%, Since _____

QUESTIONS:

1. Differentiate between voltage amplifier and power amplifier
2. Why power amplifiers are considered as large signal amplifier?
3. When does maximum power dissipation happen in this circuit?
4. What is the maximum theoretical efficiency?
5. Sketch wave form of output current with respective input signal.
6. What are the different types of class-A power amplifiers available?
7. What is the theoretical efficiency of the transformer coupled class-A power amplifier?
8. What is difference in AC, DC load line?
9. How do you locate the Q-point?
10. What are the applications of class-A power amplifier?

EXPERIMENT NO: 8

CLASS B COMPLEMENTARY SYMMETRY AMPLIFIER

AIM:

To find the efficiency of a Complementary symmetry Class B Power Amplifier.

SOFTWARE REQUIRED: Multisim

CIRCUIT DIAGRAM:

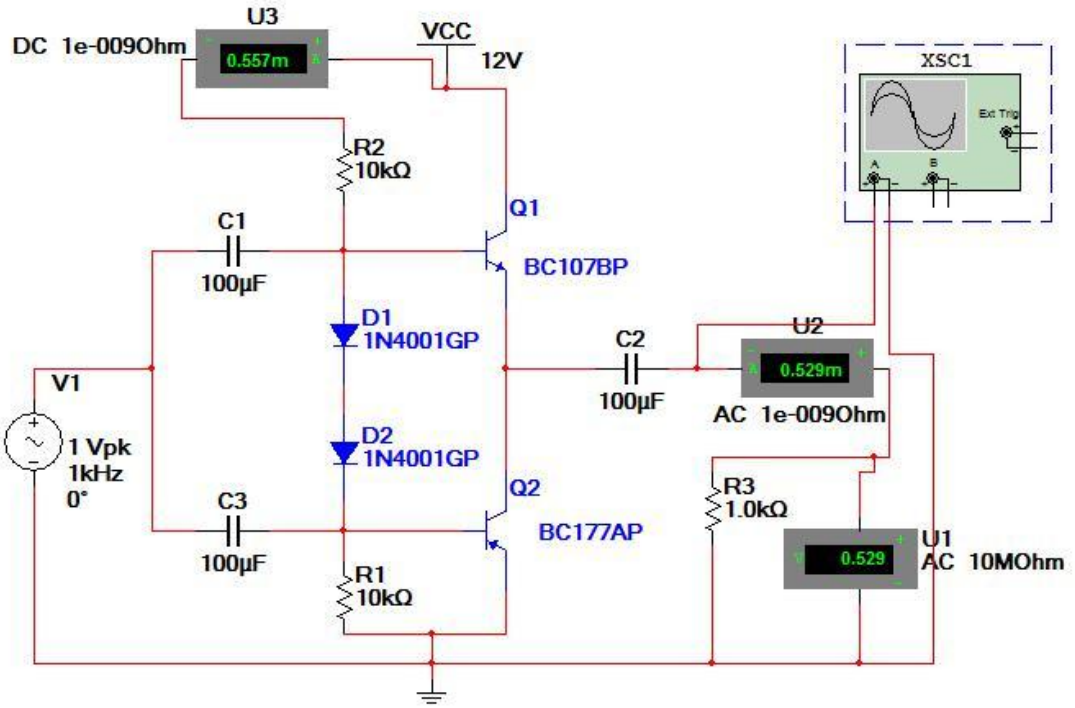


Fig1: Complementary symmetry Class B Power Amplifier Circuit With crossover distortion

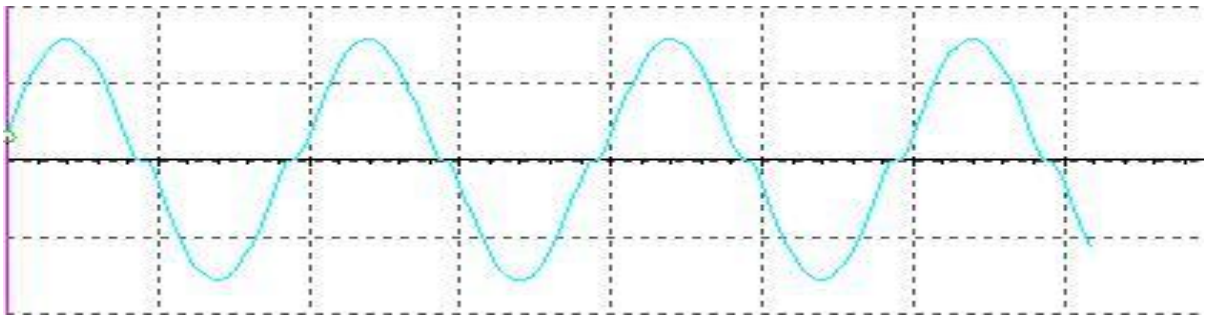


Fig 2: Output waveform of Complementary symmetry Class B Power Amplifier Circuit with crossover distortion

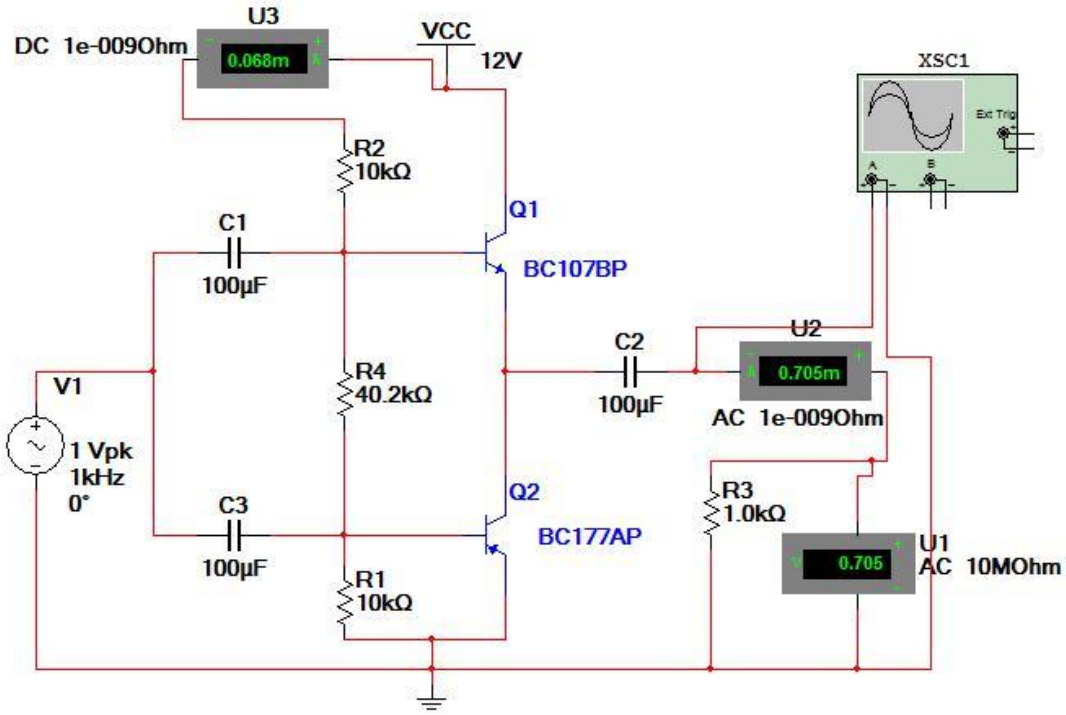


Fig 3: Class B Power Amplifier circuit Where crossover distortion is eliminated

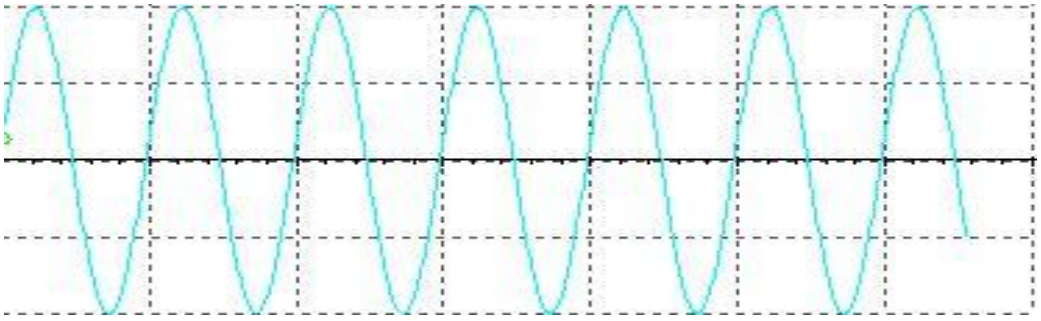


Fig 4: Output waveform of Complementary symmetry Class B Power Amplifier circuit where crossover distortion is eliminated

THEORY:

The Class B amplifier circuit above uses complimentary transistors for each half of the waveform and while Class B amplifiers have a much high efficiency than the Class A types, one of the main disadvantages of class B type push-pull amplifiers is that they suffer from an effect known commonly as Crossover Distortion.

It takes approximately 0.7 volts (measured from base to emitter) to get a bipolar transistor to start conducting. In a class B amplifier, the output transistors are not "pre -biased" to an "ON" state of operation. This means that the part of the output waveform which falls below this 0.7 volt window will not be reproduced accurately as the transition between the two transistors (when they are switching over from one to the other), the transistors do not stop or start conducting exactly at the zero crossover point even if they are specially matched pairs.

The output transistors for each half of the waveform (positive and negative) will each have a 0.7 volt area in which they will not be conducting resulting in both transistors being "OFF" at the same time.

A simple way to eliminate crossover distortion in a Class B amplifier is to add two small voltage sources to the circuit to bias both the transistors at a point slightly above their cut-off point.. However, it is impractical to add additional voltage sources to the amplifier circuit so pn-junctions are used to provide the additional bias in the form of silicon diodes.

We know that we need the base-emitter voltage to be greater than 0.7v for a silicon bipolar transistor to start conducting, so if we were to replace the two voltage divider biasing resistors connected to the base terminals of the transistors with two silicon Diodes, the biasing voltage applied to the transistors would now be equal to the forward voltage drop of the diode. These two diodes are generally called Biasing Diodes or Compensating Diodes and are chosen to match the characteristics of the matching transistors.

PROCEDURE:

1. Open the multisim icon in the system.
2. Place all the necessary components required for the design of the Complementary symmetry Class B Power amplifier circuit i.e Resistors, Capacitors, Diodes, Transistors, Voltage sources, Power sources, Ground etc on the design window.
3. Connect all the components by proper wiring and also assure that nodes are formed at the interconnection points.
4. Connect the channel of the Oscilloscope to the output of the circuit and by using the simulation switch and check output waveform.
5. To obtain the netlist, go to transfer-----►export netlist and save the netlist in a text file. On opening the text file from the saved location, a netlist is obtained containing the specifications of all the used components used in the design of the circuit.

OBSERVATIONS:

THEORETICAL CALCULATIONS :

$$I_{CQ} = V_{CC}/R_L$$

$$P_{in}\ (d.c) = V_{CC} * I_{CQ}$$

$$P_{in}(d.c) = \frac{V_{CC} * V_{CC}}{2\pi R_L} = \frac{(V_{CC})^2}{2\pi R_L}$$

$$Po(a.c) = \frac{(Vmax - Vmin) * (Imax - Imin)}{8}$$

$$(I_{max} - I_{min}) = \frac{V_{CC}}{R_L}$$

(Vmax –Vmi n) = VCC

$$Po(a.c) = \frac{V_{CC} * V_{CC}}{8R_L} = \frac{V_{CC}^2}{8R_L}$$

$$\% \text{ of efficiency} = \frac{Po(a.c)}{Pin(d.c} * 100 = \frac{V_{CC}^2/8R_L}{V_{CC}^2/2\pi R_L} * 100 = \frac{\pi}{4} * 100 = 78.5\%$$

PRACTICAL CALCULATIONS :

$$\% \text{ of efficiency} = \frac{Po(a.c)}{Pin(dc)} * 100$$

$$\eta = \frac{Pac}{Pdc} * 100$$

$$\eta = \frac{(Vac * Iac)}{(Vcc * Idc)} * 100$$

RESULT:

The efficiency of Complementary Symmetry Class B Power Amplifier is ____%.

QUESTIONS:

1.Explain complementary and symmetry concept?

2.What is the conduction angle in class B operation?

3.What is the efficiency of class B power amplifier?

4.What is the formula for output power in class B power amplifier

PART-II HARDWARE EXPERIMENTS

EXPERIMENT NO-1

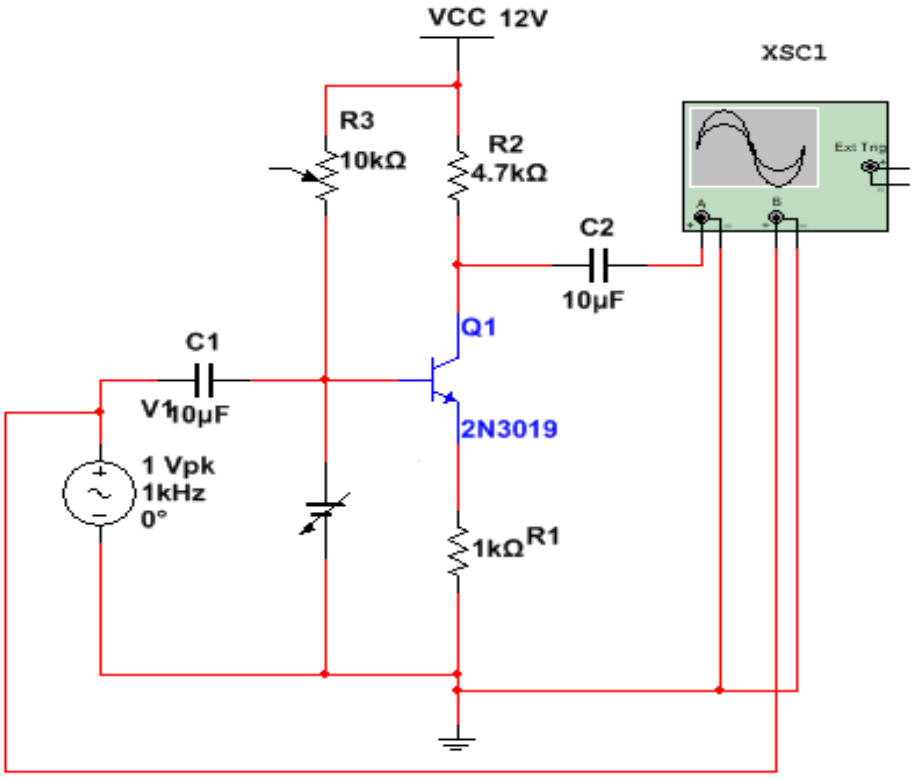
CLASS-A POWER AMPLIFIER

AIM:

To design a series fed class-A power amplifier in order to achieve max output ac power and efficiency.

EQUIPMENT REQUIRED: Class-A power amplifier kit, C.R.O, Function Generator, Connecting probes.

CIRCUIT DIAGRAM:



THEORY:

The above circuit is called as "series fed" because the load R_L is connected in series with transistor output. It is also called as direct coupled amplifier.

I_{CQ} = Zero signal collector current

V_{CEQ} = Zero signal collector to emitter voltage

Power amplifiers are mainly used to deliver more power to the load. To deliver more power it requires large input signals, so generally power amplifiers are preceded by a series of voltage amplifiers. In class-A power amplifiers, Q-point is located in the middle of DC-load line. So output current flows for complete cycle of input signal. Under zero signal condition, maximum power dissipation occurs across the transistor. As the input signal amplitude increases power dissipation reduces The maximum theoretical efficiency is 25%.

APPLICATIONS:

This is used for low power linear applications in audio and wideband RF range, where high efficiency is not required.

EXTENSIONS:

In series fed class-A power amplifier we have calculated the efficiency i.e. how efficiently DC-power is converted into AC-power depending on the magnitude of input signal. Once we design a power amplifier for a particular efficiency, the circuit will not give that efficiency to all its input signals of different amplitudes. Hence, depending on the input signal we have to choose Vcc to obtain a particular efficiency. By employing Transformer coupling, efficiency can be improved to 50%.The experiment is conducted using low power transistors like BC107, SL100 only to get familiarity in biasing and measurement. Actual power amplifiers operate at 1 watt to 100 watts. This will call for operating transistors high current and small value resistors of greater than 1/4 to 1 watt which are used in the laboratory. Actual power amplifiers use heat sinks on the transistors.

PROCEDURE:

1. Make the connections as per the circuit diagram.
2. Apply an input voltage of $1v_{p-p}$ at 1 KHz at input terminals of the circuit from the function generator.
3. Keep the input signal at constant frequency under mid frequency region and adjust the amplitude such that output voltage is undistorted and output current flows for 360^0
4. Calculate the power efficiency and compare it with theoretical efficiency.

OBSERVATIONS:

Efficiency is defined as the ratio of AC output power to DC input power

DC input power = Vcc x I_{CQ}

AC output power = $V_{P-P}^2 / 8R_L$

CALCULATIONS:

Under zero signal condition:

$Vcc = I_BR_B + V_{BE}$

$I_{BQ} = (Vcc - V_{BE}) / R_B$
$I_{CQ} = \beta \times I_{BQ}$

$V_{CE} = Vcc - I_CR_C$

EXPECTED GRAPH:

Vin=1V_{p-p}

RESULT:

1. The maximum input signal amplitude which produces undistorted output signal is _____

2. The practical efficiency of the circuit is _____

3. The efficiency observed is _____ against theoretical maximum of 25%,
Since _____

QUESTIONS:

1. Differentiate between voltage amplifier and power amplifier
2. Why power amplifiers are considered as large signal amplifier?
3. When does maximum power dissipation happen in this circuit?
4. What is the maximum theoretical efficiency?
5. Sketch wave form of output current with respective input signal.
6. What are the different types of class-A power amplifiers available?
7. What is the theoretical efficiency of the transformer coupled class-A power amplifier?
8. What is difference in AC, DC load line?
9. How do you locate the Q-point?
10. What are the applications of class-A power amplifier?

EXPERIMENT NO:2

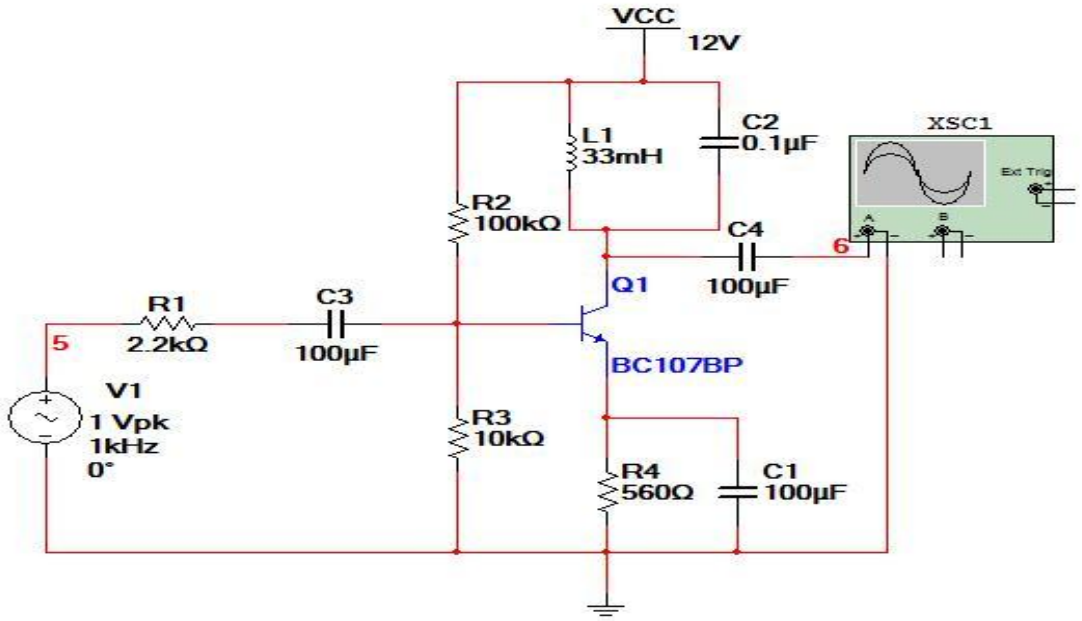
SINGLE TUNED VOLTAGE AMPLIFIER

AIM:

To determine the resonant frequency and bandwidth of a tuned amplifier.

EQUIPMENT REQUIRED: Tuned voltage amplifier kit, Function generator, CRO, connecting probes.

CIRCUIT DIAGRAM:



THEORY:

A tuned amplifier is one which uses one or more parallel tuned circuit as the load impedance.A tuned amplifier is capable of amplifying a signal over a narrow band of frequencies.The gain of a tuned amplifier is maximum at the resonant frequency and it falls sharply below and above the resonant frequency. At the resonant frequency, the inductive and capacitive reactances are equal.

$f_o = 1/ 2\pi \sqrt{(LC)}$

PROCEDURE:

1. Apply an input voltage of 1vp -p at 1 kHz from the function generator at the input terminals of the Tuned voltage amplifier and observe the signal on the CRO.
2. Connect the output of the circuit to the channel of the CRO.
3. Note down the output voltage.
4. Calculate the voltage gain in dB using the formula Av=20 log (Vo/Vi).

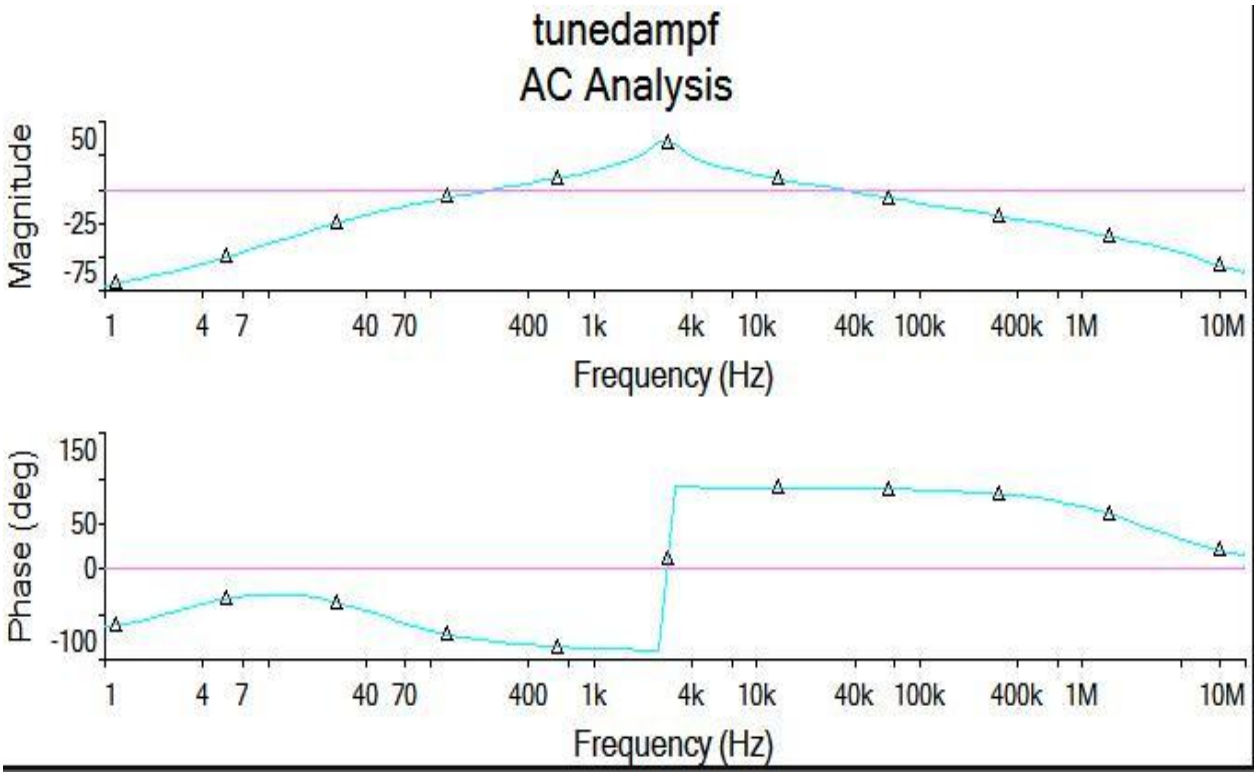
OBSERVATION TABLE:

S.NO	FREQUENCY(Hz)	GAIN(dB)

Bandwidth of the Tuned amplifier=f_h-f_l Hz

EXPECTED GRAPH:

Frequency response and phase response graphs



RESULT:

The maximum gain is _____dB, the resonant frequency is _____Hz and bandwidth is _____Hz of the Tuned Amplifier.

QUESTIONS:

1. What is a tuned amplifier?
2. What is the formula for resonant frequency of a tuned amplifier?
3. What is the difference between single, double and stagger tuned amplifiers?

EXPERIMENT NO-3 (A)

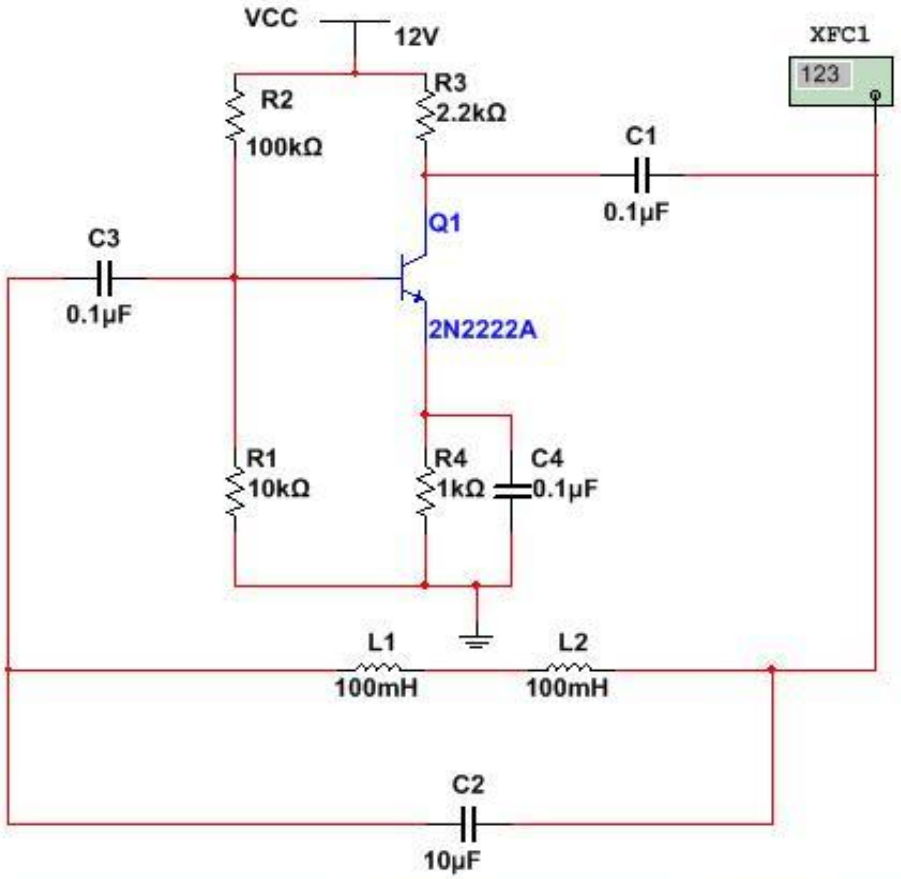
HARTLEY OSCILLATOR

AIM:

To determine the frequency of oscillation of the Hartley Oscillator.

EQUIPMENT REQUIRED: Hartley Oscillator kit, CRO, Connecting probes.

CIRCUIT DIAGRAM:



THEORY:

The Hartley oscillator is distinguished by a tank circuit consisting of two series-connected coils in parallel with a capacitor, with the feedback signal needed for oscillation taken from the center connection between the coils; the coils act as a voltage divider. The Hartley oscillator is the dual of the Colpitts oscillator which uses a voltage divider made of two capacitors rather than two inductors. Although there is no requirement for there to be mutual coupling between the two coil segments, the circuit is usually implemented using a tapped coil, with the feedback taken from the tap, as shown here. The optimal tapping point (or ratio of coil inductances) depends on the amplifying device used, which may be a bipolar junction transistor, FET, triode, or amplifier of almost any type (non-inverting in this case, although variations of the circuit with an earthed centre-point and feedback from

an inverting amplifier or the collector/drain of a transistor are also common), but a Junction FET (shown) or triode is often employed as a good degree of amplitude stability (and thus distortion reduction) can
be achieved with a simple grid leak resistor-capacitor combination in series with the gate or grid (see the Scott circuit below) thanks to diode conduction on signal peaks building up enough negative bias to limit amplification.

The frequency of oscillation is approximately the resonant frequency of the tank circuit. If the capacitance of the tank capacitor is *C* and the total inductance of the tapped coil is *L* then

$$f = \frac{1}{2\pi\sqrt{LC}}$$

If two *uncoupled* coils of inductance L_1 and L_2 are used then

$$L = L_1 + L_2$$

However if the two coils are magnetically coupled the total inductance will be greater because of mutual inductance k[1]

$$L = L_1 + L_2 + k\sqrt{L_1 L_2}$$

The actual oscillation frequency will be slightly lower than given above, because of parasitic capacitance in the coil and loading by the transistor.

Advantages of the Hartley oscillator include:

1. The frequency may be adjusted using a single variable capacitor, one side of which can be earthed
2. The output amplitude remains constant over the frequency range
3. Either a tapped coil or two fixed inductors are needed, and very few other components
4. Easy to create an accurate fixed-frequency Crystal oscillator variation by replacing the capacitor with a (parallel-resonant) quartz crystal or replacing the top half of the tank circuit with a crystal and grid-leak resistor (as in the Tri-tet oscillator).

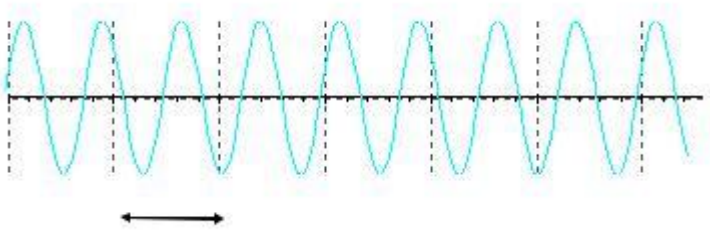
Disadvantages include:

Harmonic-rich output if taken from the amplifier and not directly from the LC circuit (unless amplitude - stabilization circuitry is employed).

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Connect the output of the Hartley Oscillator kit to the CRO.
3. Observe the sinusoidal signal as an output and note down the time period of the oscillation.
4. Compare the practical frequency with the theoretical frequency.

EXPECTED GRAPH:



T

OBSERVATIONS:

i. Theoretical frequency of oscillation:

L1= L2= C=

$$L = L_1 + L_2$$

$$f = \frac{1}{2\pi\sqrt{LC}}$$

ii. Practical frequency of oscillation:

T= _____

fo=1/ T= _____Hz

RESULT: The theoretical and practical frequency of oscillation of the Hartley Oscillator is calculated as _____ and _____.

EXPERIMENT NO-3 (B)

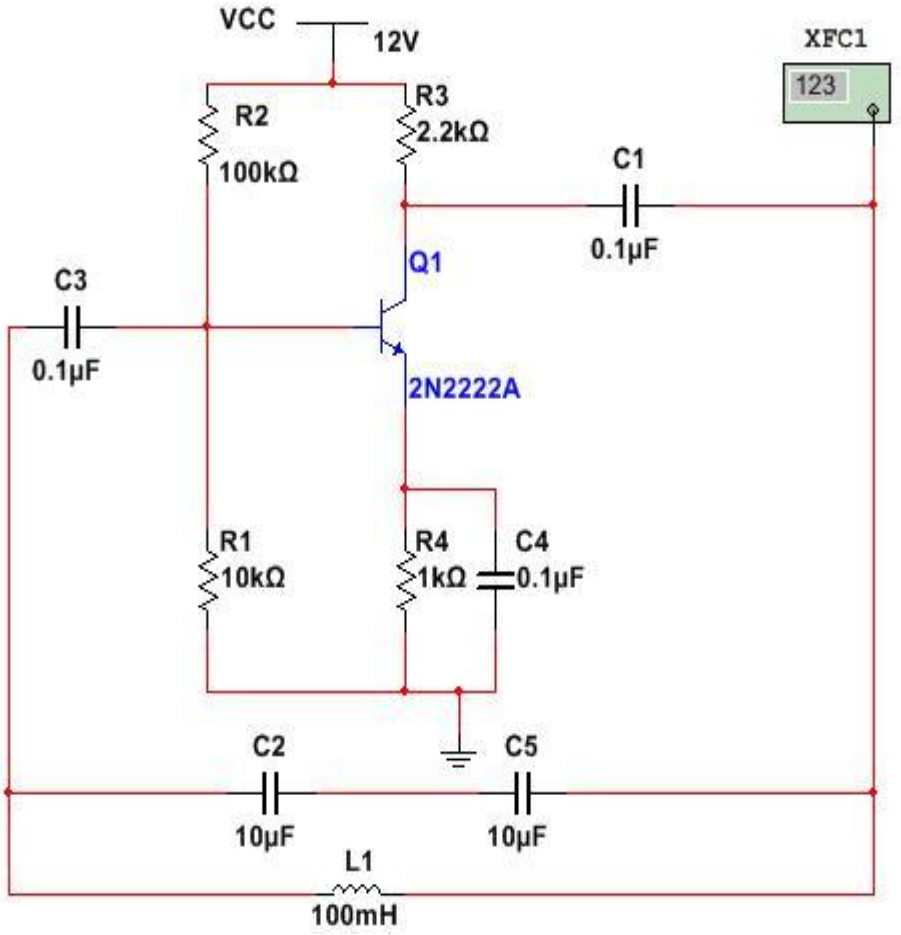
COLPITTS OSCILLATOR

AIM:

To determine the frequency of oscillation of a Colpitts Oscillator

EQUIPMENT REQUIRED: Colpitts Oscillator kit, CRO, Connecting probes

CIRCUIT DIAGRAM:



THEORY:

The Colpitts circuit, like other LC oscillators, consists of a gain device (such as a bipolar junction transistor, field effect transistor, operational amplifier, orvacuum tube) with its output connected to its input in a feedback loopcontaining a parallel LC circuit (tuned circuit) which functions as a bandpass filter to set the frequency of oscillation.

Colpitts oscillator is the electrical dual of a Hartley oscillator, where the feedback signal is taken from an "inductive" voltage divider consisting of two coils in series (or a tapped coil). Fig. 1 shows the common-base Colpitts circuit. L and the series combination of C_1 and C_2 form the parallel resonant tank circuit which determines the frequency of the oscillator. The voltage across C_2 is applied

to the base-emitter junction of the transistor, as feedback to create oscillations. Fig. 2 shows the common-collector version.

Here the voltage across C_1 provides feedback. The frequency of oscillation is approximately the resonant frequency of the LC circuit, which is the series combination of the two capacitors in parallel with the inductor.

$$f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1 C_2}{C_1+C_2}\right)}}$$

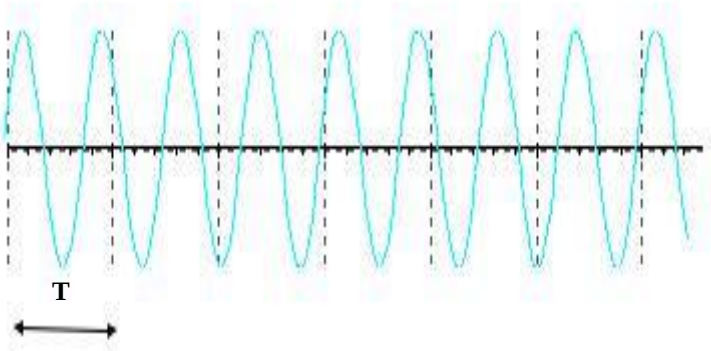
The actual frequency of oscillation will be slightly lower due to junction capacitances and resistive loading of the transistor.

As with any oscillator, the amplification of the active component should be marginally larger than the attenuation of the capacitive voltage divider, to obtain stable operation. Thus, a Colpitts oscillator used as a variable frequency oscillator (VFO) performs best when a variable inductance is used for tuning, as opposed to tuning one of the two capacitors. If tuning by variable capacitor is needed, it should be done via a third capacitor connected in parallel to the inductor (or in series as in the Clapp oscillator).

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Connect the output of the Colpitts Oscillator kit to the CRO.
3. Observe the sinusoidal signal as an output and note down the time period of the oscillation.
4. Compare the practical frequency with the theoretical frequency.

EXPECTED GRAPH:



OBSERVATIONS:

I. THEORETICAL FREQUENCY OF OSCILLATION:

C1= C2= L=

$$f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1C_2}{C_1+C_2}\right)}}$$

II. PRACTICAL FREQUENCY OF OSCILLATION: T= _____

fo =1/ T= _____Hz

RESULT: The theoretical and practical frequency of oscillation of the Colpitts Oscillator is calculated as _____ and _____.

QUESTIONS:

1. What is an Oscillator?
2. What is the main difference between an amplifier and an oscillator?
3. State Barkhausen criterion for oscillation.
4. State the factors on which oscillators can be classified.
5. What are the factors which contribute to change in frequency in oscillators?

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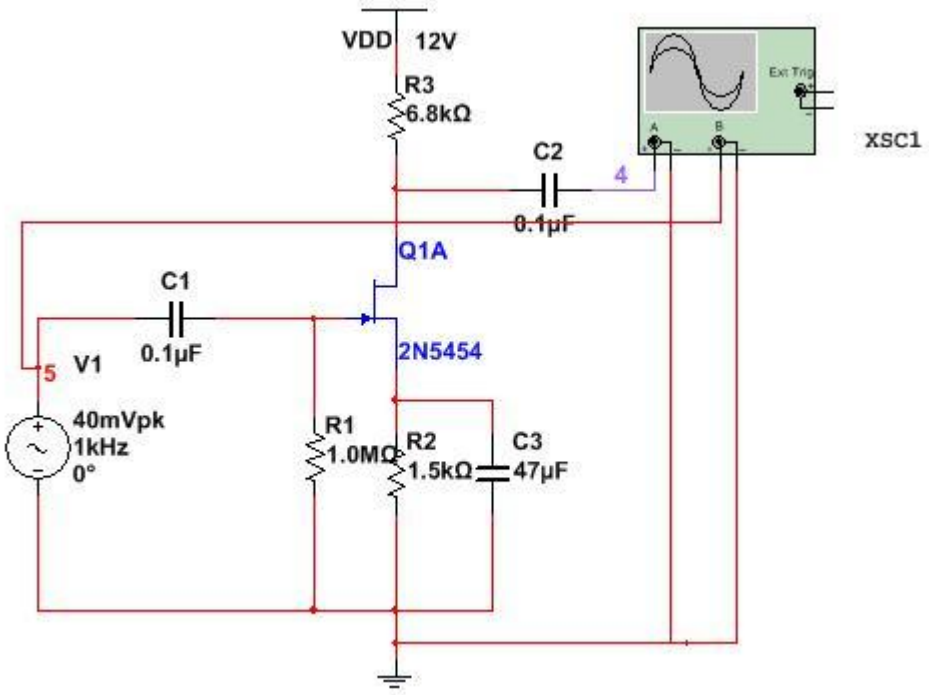
EXPERIMENT NO-4

COMMON SOURCE AMPLIFIER

AIM: To determine the Bandwidth from the frequency response of the Common Source FET Amplifier.

HARDWARE REQUIRED: common source hardware kit, function generator, CRO, Connecting probes

CIRCUIT DIAGRAM:



THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain.

The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide- semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes.

In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P -N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate.

However, under some conditions there is a small current through the junction during part of the input signal cycle. The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes. A common source amplifier FET amplifier has high input impedance and a moderate voltage gain. Also, the input and output voltages are 180 degrees out of Phase.

PROCEDURE:

1. Apply an input voltage of 40mvp-p at 1 kHz from the function generator at the input terminals of the common source amplifier and observe the signal on the CRO.
2. Connect the output of the common source amplifier to the other channel of the CRO.
3. Vary the input frequency from 10Hz to 1MHz with input voltage constant (40mvpp) and note down the output voltage.
4. Calculate the voltage gain in dB using the formula Av=20 log (Vo/vi)

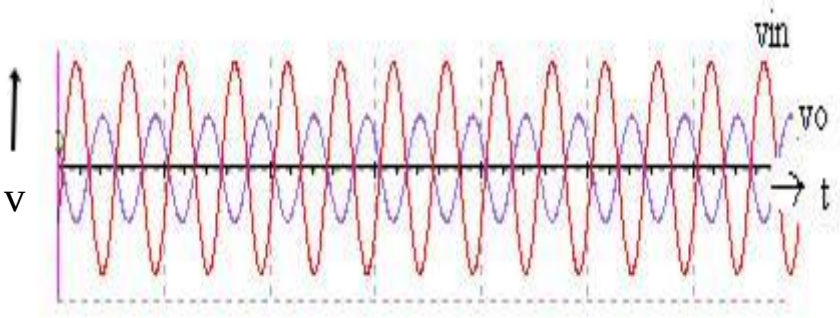
OBSERVATION TABLE:

S.NO	FREQUENCY(Hz)	GAIN(dB)

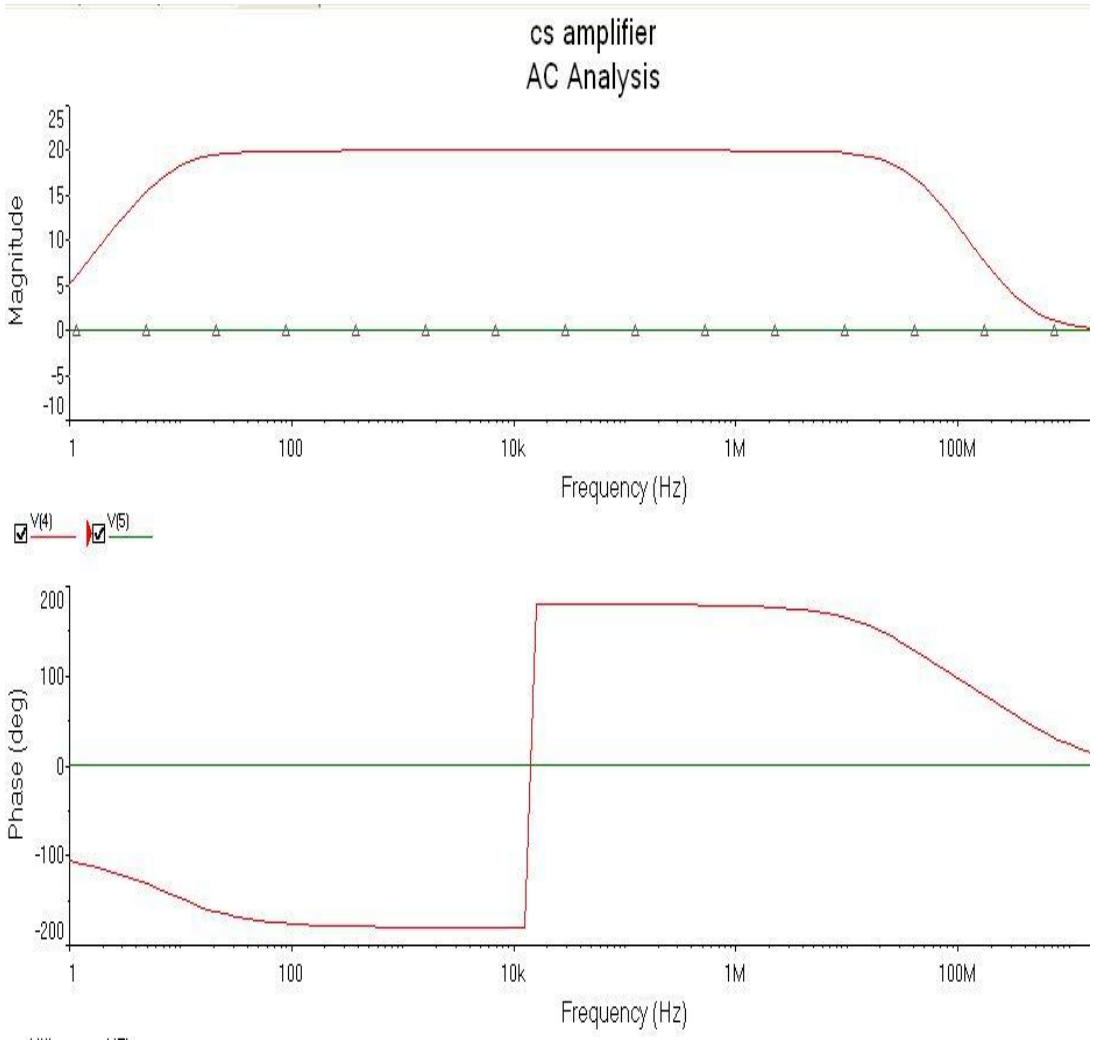
Bandwidth of the CE-CB Cascode amplifier=f_h-f_l Hz

MODEL GRAPH:

INPUT VS OUTPUT WAVEFORMS



FREQUENCY RESPONSE:



RESULT:We have obtained the frequency response of the common Source Amplifier and also found its Bandwidth to be _____Hz.

QUESTIONS:

1. How does FET acts as an amplifier?
2. What are the parameters of a FET?
3. What is an amplification factor?
4. Draw the h-parameter model of the FET.
5. What are the advantages of FET over BJT?
6. What is the region of FET so that it acts as an amplifier?
7. What are the differences between JFET and MOSFET?
8. What type of biasing is used in the given circuit?

APPENDIX-A

QUESTIONARE

MIDBAND ANALYSIS OF SMALL SIGNAL AMPLIFIERS

1. What do you understand by Operating point?
2. Why do we choose the Q point at the center of the load line?
3. Name the two techniques used in the stability of the q point .explain.?
4. Define stability factor &Give the expression for stability factor?
5. List out the different types of biasing.
6. What do you meant by thermal runway?
7. Why transistor is called as a current controlled device?
8. Define current amplification factor?
9. What are the requirements for biasing circuits?
10. When does a transistor act as a switch?
11. What is biasing?
12. What is an operating point?
13. What is d.c load line?
14. Explain about the various regions in a transistor?
15. Explain about the characteristics of a transistor?
16. Why the operating point is selected at the Centre of the active region?
17. What is an amplifier?
18. What is small signal amplifier?
19. What is a Darlington pair?
20. What are the advantages of double tuned over single tuned?

FREQUENCY RESPONSE OF AMPLIFIERS

1. Draw a hybrid model for a BJT.
2. What is the relationship between bandwidth and rise time?
3. What are the high frequency effects?
4. If the rise time of a BJT is 35 nano seconds, what is the bandwidth that can be obtained using this BJT?
5. Explain the usefulness of the decibel unit.
6. Define the term bandwidth of an amplifier?
7. State various capacitances in the hybrid model?
8. Define the term bandwidth of an amplifier?
9. Why it is not possible to use the h- parameters at high frequencies?
10. What do you mean by the half power or 3 db frequencies?

UNTUNED AMPLIFIERS

1. What is an effect of cascading?
2. What are all the factors affecting the bandwidth of the RC Coupled amplifiers
3. Explain bypass capacitor?
4. What is meant by coupling capacitor?
5. Why does amplifier gain reduce?
6. Explain the different regions in frequency response?
7. State the types of distortions in amplifier?
8. What is cross over distortion? How it can be eliminated?
9. Define noise?
10. Define step response?

FEEDBACK AMPLIFIER AND OSCILLATORS

1. What is feedback and what are feedback amplifiers?
2. What is meant by positive and negative feedback?
3. What are the advantages and disadvantages of negative feedback?
4. Differentiate between voltage and current feedback in amplifiers?
5. Define sensitivity?
6. Define De-sensitivity?
7. What is the type of feedback used in an op- amp Schmitt trigger?
8. Give the expression for the frequency of oscillations in an op-amp sine wave Oscillator?
9. What are the conditions for sustained oscillator or what is Barkhausene's criterion?
10. What is Oscillator circuit?
11. What are the classifications of Oscillators?
12. What are the types of feedback oscillators?
13. Define Piezo-electric effect?
14. Draw the equivalent circuit of crystal oscillator?
15. What is Miller crystal oscillator? Explain its operation?
16. State the frequency for RC phase shift oscillator?
17. Give the topology of current amplifier with current shunt feedback?
18. What are gain margin and phase margin?
19. What is the minimum value of hfe for the oscillations in transistorized RC Phase shift oscillator?
20. What is LC oscillator?

LARGE SIGNAL AMPLIFIERS

1. What is class AB operation?
2. Define conversion efficiency of a power amplifier. What is its value for class C power amplifier?
3. What is crossover distortion? How it can be eliminated?
4. What is meant by Harmonic distortion?
5. What is the drawback of class B amplifier? How is this minimized?
6. Define thermal resistance in the context of power amplifier.
7. What are the types of class B amplifier?
8. Draw a quasi complimentary symmetry power amplifier?
9. What is the advantage of using the output transformer for a class A amplifier?
10. What is the disadvantage of transformer coupled class A amplifier?

EXPERIMENT NO-1

LINEAR WAVE SHAPING

AIM:

i) To design a low pass RC circuit for the given cutoff frequency and obtain its frequency response.

ii) To observe the response of the designed low pass RC circuit for the given square waveform for T<<RC, T=RC and T>>RC.

iii) To design a high pass RC circuit for the given cutoff frequency and obtain its frequency response**.**

iv) To observe the response of the designed high pass RC circuit for the given square waveform for T<<RC, T=RC and T>>RC.

APPARATUS REQUIRED:

Name of the Component/Equipment	Specifications	Quantity
Resistors	1KΩ	1
	2.2KΩ,16 KΩ	1
Capacitors	0.01μF	1
CRO	20MHz	1
Function generator	1MHz	1

THEORY:

The process whereby the form of a non sinusoidal signal is altered by transmission through a linear network is called "linear wave shaping"

An ideal low pass circuit is one that allows all the input frequencies below a frequency called cutoff frequency f_c and attenuates all those above this frequency. For practical low pass circuit (Fig.1) cutoff is set to occur at a frequency where the gain of the circuit falls by 3 dB from its maximum at very high frequencies the capacitive reactance is very small, so the output is almost equal to the input and hence the gain is equal to 1. Since circuit attenuates low frequency signals and allows high frequency signals with little or no attenuation, it is called a high pass circuit.

CIRCUIT DIAGRAM:

LOW PASS RC CIRCUIT :

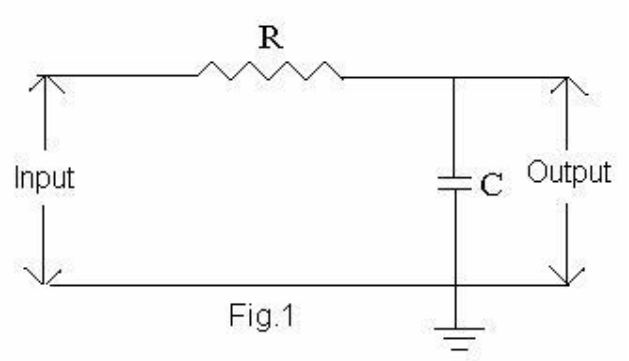


Fig.1

HIGH PASS RC CIRCUIT :

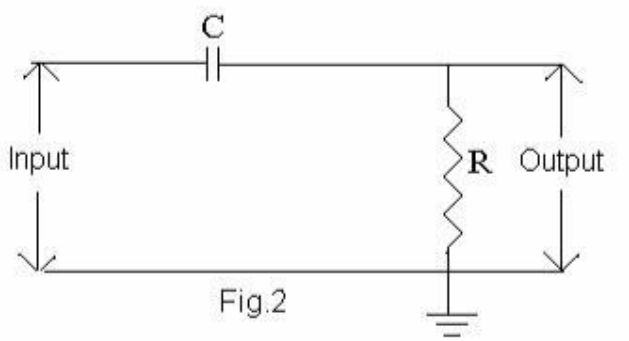


Fig.2

PROCEDURE:

A) Frequency response characteristics:

1. 1 .Connect the circuit as shown in Fig.1 and apply a sinusoidal signal of amplitude of 2V p-p as input.
2. Vary the frequency of input signal in suitable steps 100 Hz to 1 MHz and note down the p-p amplitude of output signal.
3. Obtain frequency response characteristics of the circuit by finding gain at each
4. Frequency and plotting gain in dB vs frequency .
5. Find the cutoff frequency f_c by noting the value of f at 3 dB down from the maximum gain

B) Response of the circuit for different time constants:

Time constant of the circuit RC= 0.0198 ms

1. Apply a square wave of 2v p-p amplitude as input.
2. Adjust the time period of the waveform so that T>>RC, T=RC, T<<RC and observe the output in each case.
3. Draw the input and output wave forms for different cases.

Sample readings

Low Pass RC Circuit

Input Voltage: V_i=2 $V_{(p-p)}$

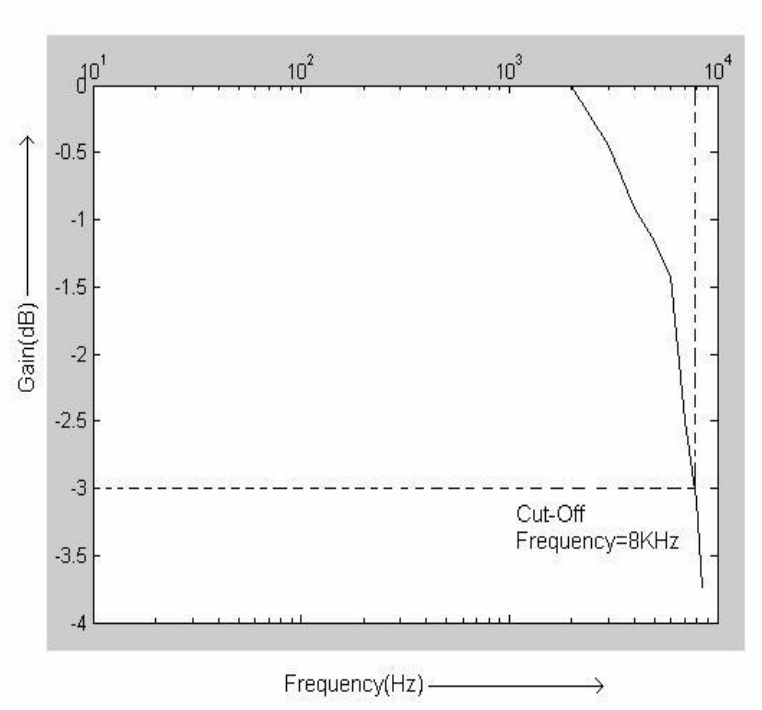
S.No	Frequency (Hz)	O/P Voltage, V_o (V)	Gain = 20log(Vo/Vi) (dB)
1	100		
2	200		
3	500		
4	1k		
5	2k		
6	3k		
7	4k		
8	5k		
9	6k		
10	7k		
11	8k		

High Pass RC Circuit:

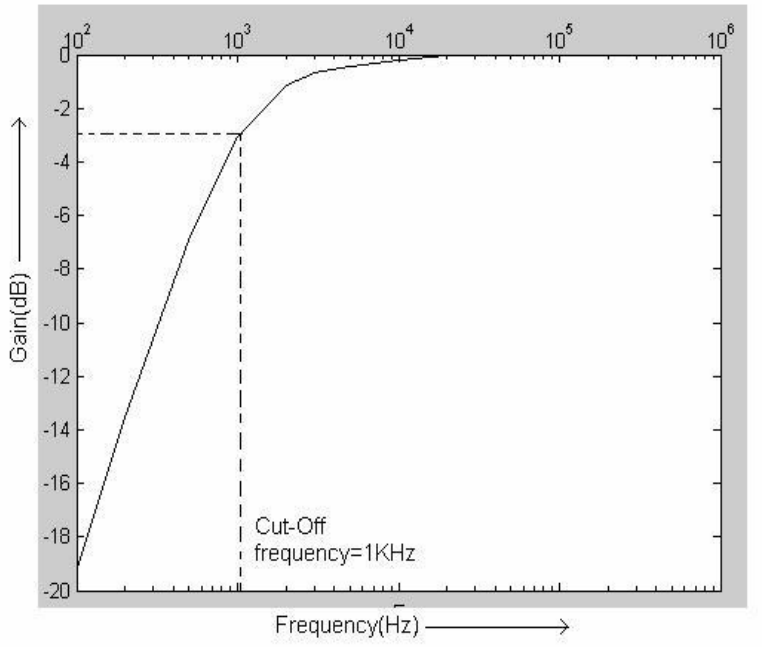
S.No	Frequency(Hz)	O/P Voltage, V_o (V)	Gain = 20log(Vo/Vi) (dB)
1	100Hz		
2	200Hz		
3	300Hz		
4	500Hz		
5	700Hz		
6	900Hz		
7	1KHz		
8	3KHz		
9	5KHz		
10	7KHz		
11	9KHz		
12	10KHz		
13	70KHz		
14	100KHz		
15	300KHz		
16	500KHz		
17	700KHz		
18	1MHz		

MODEL GRAPHS AND WAVE FORMS:

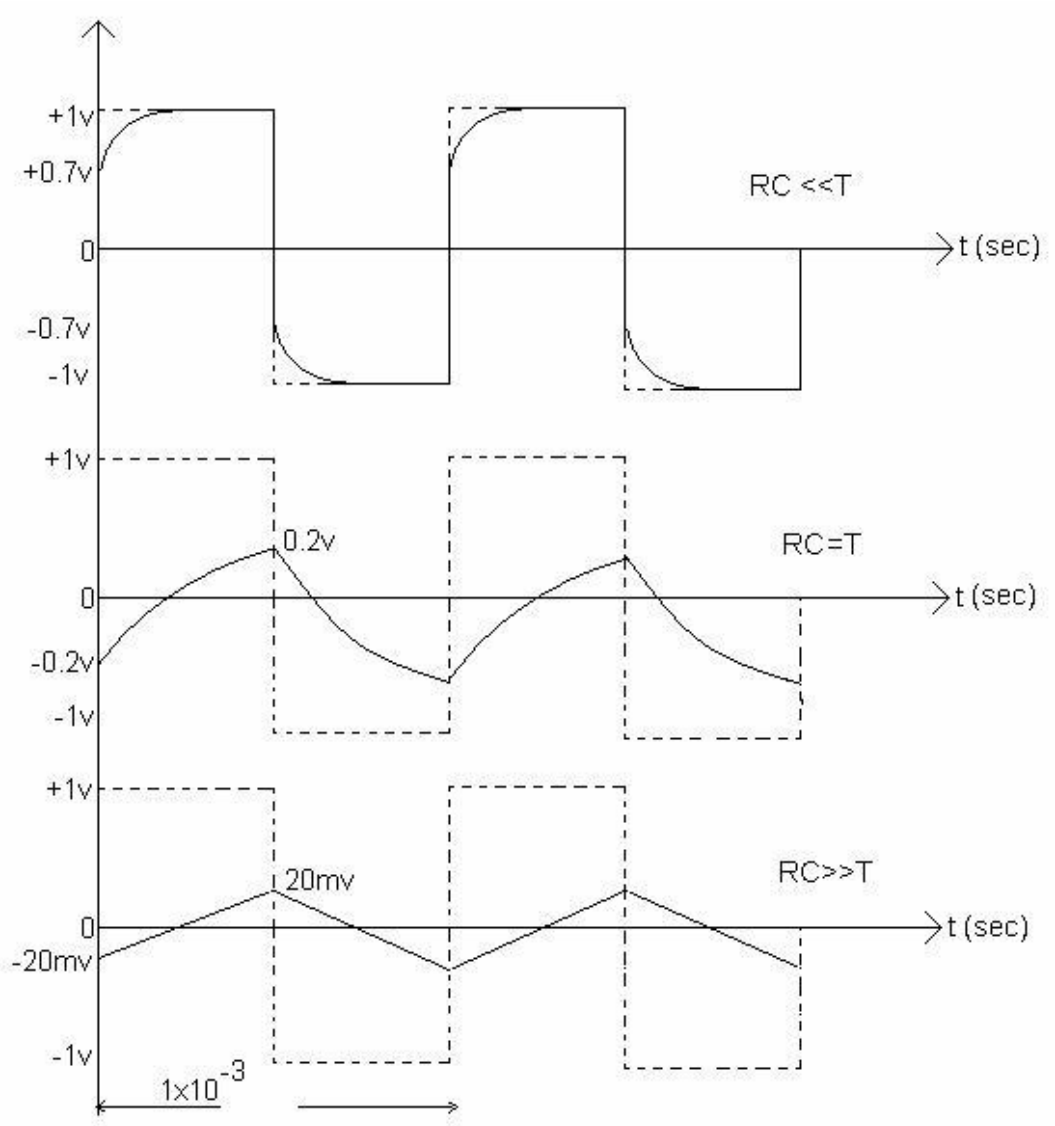
LOW PASS RC CIRCUIT FREQUENCY RESPONSE:



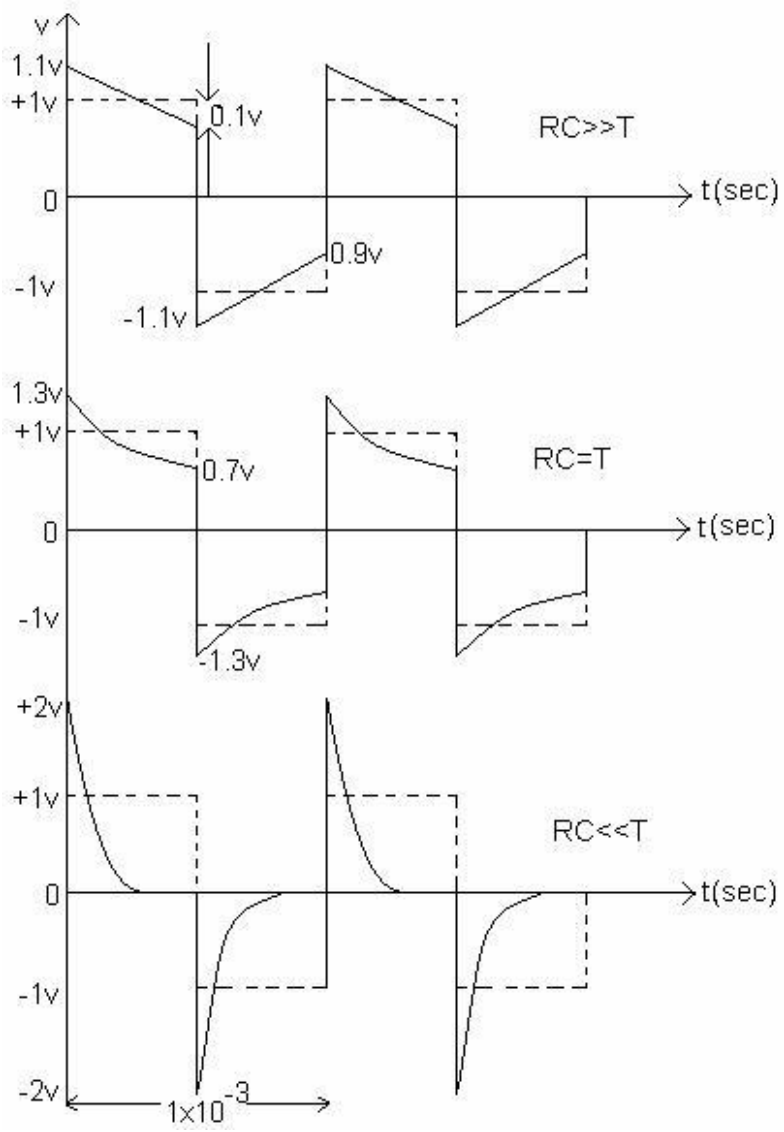
HIGH PASS RC CIRCUIT FREQUENCY RESPONSE:



LOW PASS RC CIRCUIT:



HIGH PASS RC CIRCUIT:



PRECAUTIONS:

1. Connections should be made carefully**.**
2. Verify the circuit connections before giving supply.
3. Take readings without any parallax error.

Result:

RC low pass and high pass circuits are designed, frequency response and response at different time constants is observed.

Inference:

At low frequencies the capacitor C behaves almost like a open circuit and output is equal to input voltage. As the frequency increases the reactance of the capacitor increases and C functions almost like a short circuit and output voltage is equal to zero.

Questions & Answers:

1. Define linear wave shaping?

Ans. The process whereby the form of a non-sinusoidal signal is altered by transmission through a linear network is called linear wave shaping.

2. When does the low pass circuit act as integrator?

Ans. When the time constant of an RC low-pass circuit is very large in comparison with the time required for the input signal to make an appreciable change, the circuit acts as an integrator.

3. When does the high pass circuit acts as a differentiator?

Ans. The high-pass RC circuit acts as a differentiator provided the RC constant of the circuit is very small in comparison with that required for the input signal to make an appreciable change.

EXPERIMENT NO-2(A)

NON LINEAR WAVE SHAPPING-CLIPPERS

AIM:

To obtain the output and transfer characteristics of various diode clipper circuits.

APPARATUS REQUIRED:

Name of the Component/Equipment	Specifications	Quantity
Resistors	1KΩ	1
Diode	1N4007	1
CRO	20MHz	1
Function generator	1MHz	1
DC Regulated power supply	0-30V,1A	1

THEORY:

The basic action of a clipper circuit is to remove certain portions of the waveform, above or below certain levels as per the requirements. Thus the circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or Clippers. The half wave rectifier is the best and simplest type of clipper circuit which clips off the positive/negative portion of the input signal. The clipper circuits are also called limiters or slicers.

CIRCUIT DIAGRAMS:

POSITIVE PEAK CLIPPER WITH REFERENCE VOLTAGE, V=2V

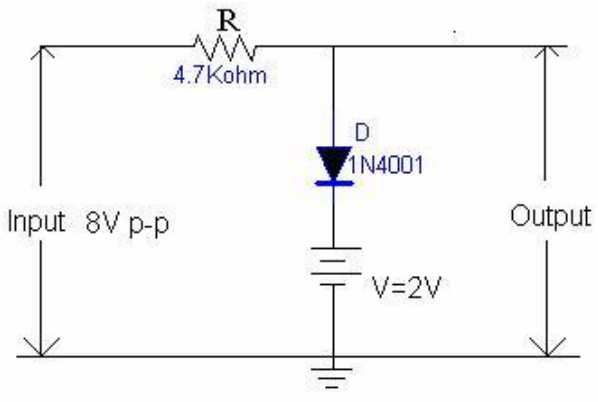


Fig.1

POSITIVE BAISE CLIPPER WITH REFERENCE VOLTAGE, V=2V

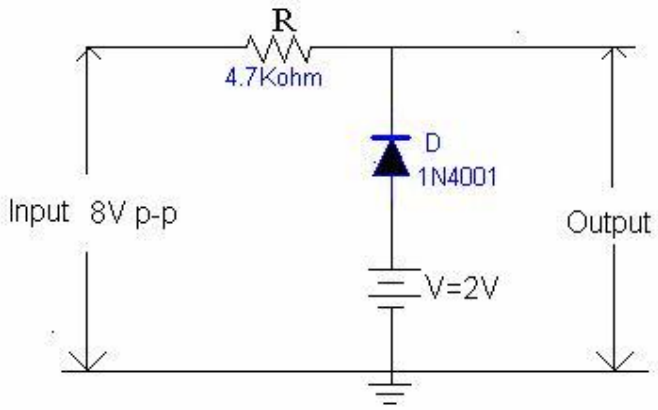


Fig.2

NEGATIVE BAISE CLIPPER WITH REFERENCE VOLTAGE, V=-2V

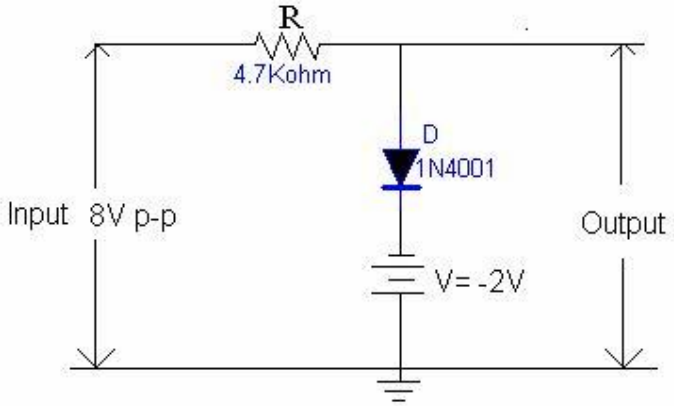


Fig.3

NEGATIVE PEAK CLIPPER WITH REFERENCE VOLTAGE, V=-2V

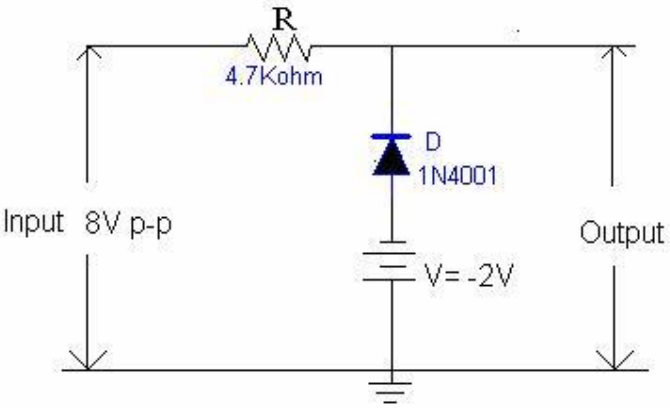


Fig.4

CLIPPING AT TWO INDEPENDENT LEVELS:(SLICCER)

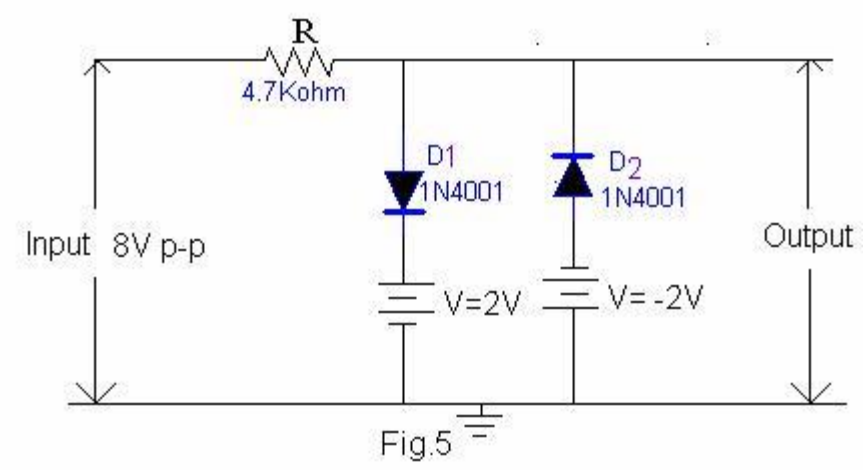


Fig.5

PROCEDURE:

1. Connect the circuit as per circuit diagram shown in Fig.1
2. Obtain a sine wave of constant amplitude 8 V p-p from function generator and apply as input to the circuit.
3. Observe the output waveform and note down the amplitude at which clipping occurs.Draw the observed output waveforms.
4. To obtain the transfer characteristics apply dc voltage at input terminals and vary the voltage insteps of 1V up to the voltage level more than the reference voltage and note down the corresponding voltages at the output.
5. Plot the transfer characteristics between output and input voltages.
6. Repeat the steps 1 to 5 for all other circuits.

SAMPLE READINGS:

POSITIVE PEAK CLIPPER: REFERENCE VOLTAGE, V=2V

S.No	I/p voltage (v)	O/p voltage (v)
1	-6	
2	-5	
3	-4	
4	-3	
5	-2	
6	-1	
7	0	
8	1	
9	2	
10	3	
11	4	
12	5	
13	6	

POSITIVE BAISE CLIPPER: REFERENCE VOLTAGE V= 2V

S.No	I/p voltage(v)	O/p voltage(v)
1	-6	
2	-5	
3	-4	
4	-3	
5	-2	
6	-1	
7	0	
8	1	
9	2	
10	3	
11	4	
12	5	
13	6	

NEGATIVE BAISE CLIPPER: REFERENCE VOLTAGE V=2V

S.No	I/P voltage(v)	O/P voltage(v)
1	-6	
2	-5	
3	-4	
4	-3	
5	-2	
6	-1	
7	0	
8	1	
9	2	

NEGATIVE PEAK CLIPPER: REFERENCE VOLTAGE V= 2V

S.No	I/P voltage(v)	O/P voltage(v)
1	-6	
2	-5	
3	-4	
4	-3	
5	-2	
6	-1	
7	0	
8	1	
9	2	
10	3	
11	4	
12	5	
13	6	

SLICER :

S.No	I/p voltage(v)	O/p voltage(v)
1	-6	
2	-5	
3	-4	
4	-3	
5	-2	
6	-1	
7	0	
8	1	
9	2	
10	3	
11	4	
12	5	
13	6	

THEORETICAL CALCULATIONS:

Positive peak clipper:

V_r=2v, Vγ=0.6v

When the diode is forward biased $V_o = V_r + V\gamma = 2.6v$

When the diode is reverse biased the $V_o=V_i$

Positive base clipper:

V_r=2v, Vγ=0.6v

When the diode is forward biased Vo=Vr –Vγ = 1.4v

When the diode is reverse biased $V_o=V_i$.

Negative base clipper:

V_r=2v, Vγ=0.6v

When the diode is forward biased $V_o = -V_r + V\gamma = -1.4v$

When the diode is reverse biased $V_o=V_i$.

Negative peak clipper:

V_r=2v, Vγ=0.6v

When the diode is forward biased V_o= -(V_r+ Vγ) =-2.6v

When the diode is reverse biased V_o=V_i .

Slicer:

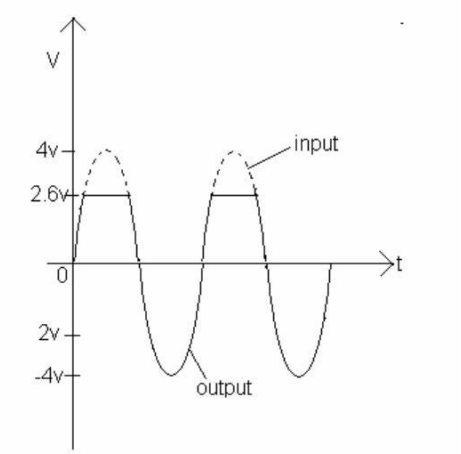
When the diode D1 is forward biased and D2 is reverse biased V_o= V_r+ V γ =2.6v

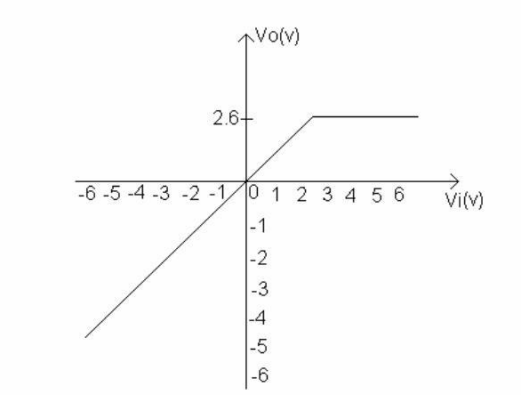
When the diode D2 is forward biased and D2 is reverse biased V_o=-(V_r+ Vγ) =-2.6v

When the diodes D1 D2 are reverse biased V_o=V_i .

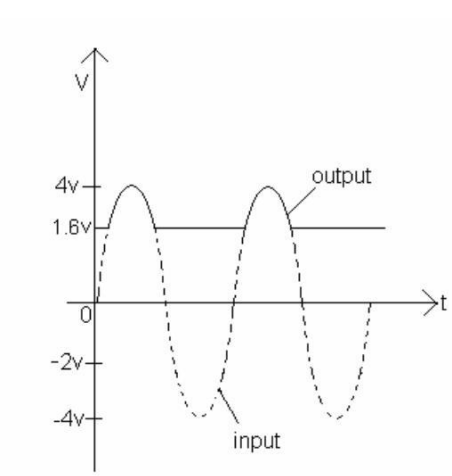
MODEL WAVE FORMS AND TRANSFER CHARACTERISTICS

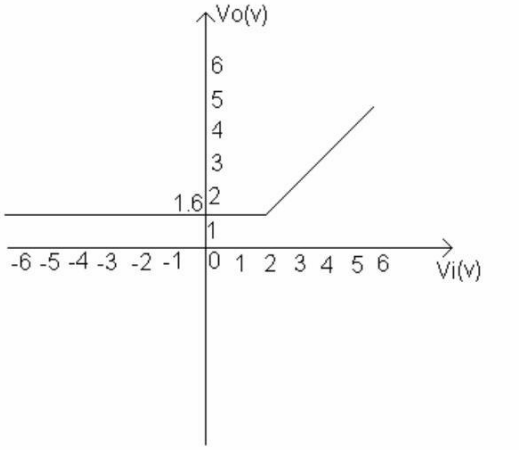
POSITIVE PEAK CLIPPER: REFERENCE VOLTAGE V=2V



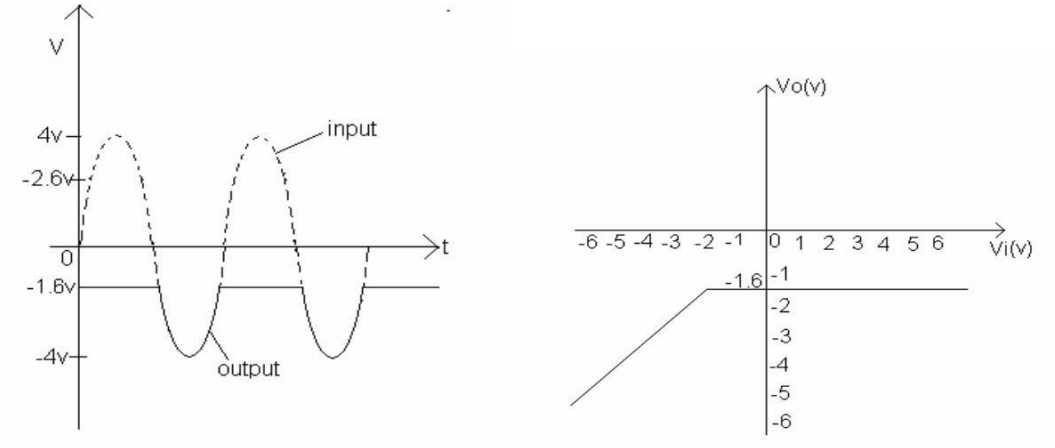


POSITIVE BASE CLIPPER: REFERENCE VOLTAGEV=2V

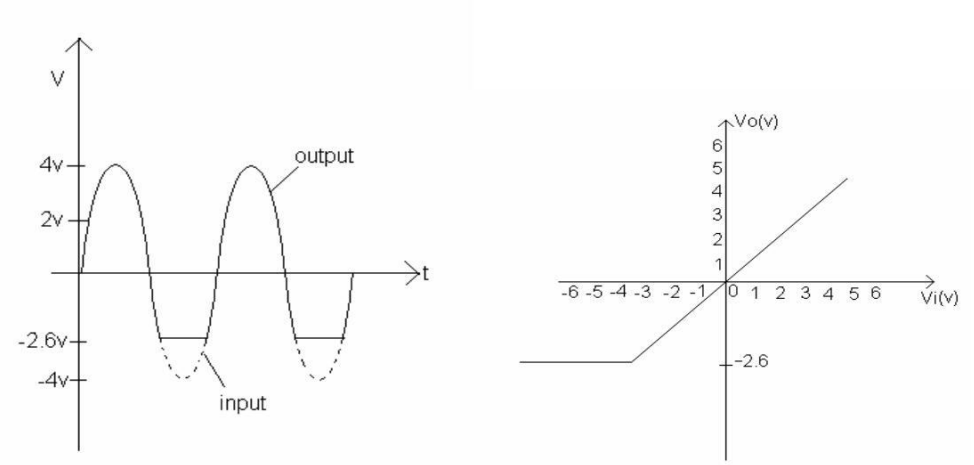




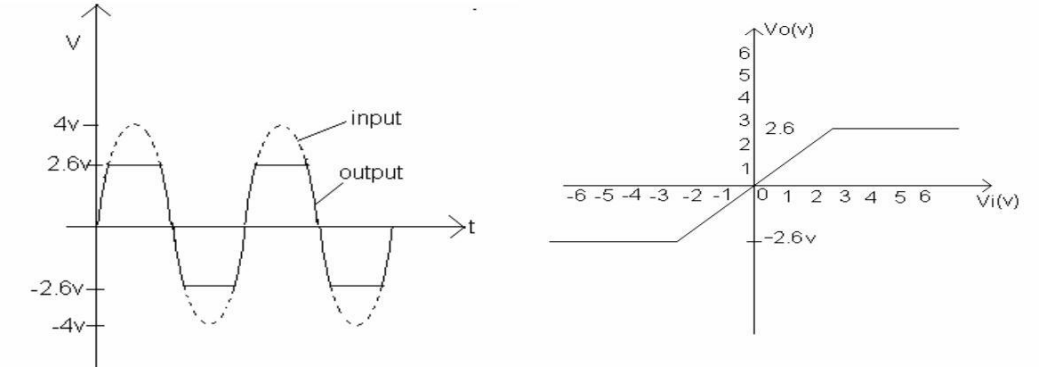
NEGATIVE BASE CLIPPER: REFERENCE VOLTAGE V=2V



NEGATIVE PEAK CLIPPER: REFERENCE VOLTAGE V=2V



SLICER CIRCUIT:



PRECAUTIONS:

1. Connections should be made carefully**.**
2. Verify the circuit before giving supply.
3. Take readings without any parallax error.

RESULT:

Performance of different clipping circuits is observed and their transfer characteristics are obtained.

INFERENCE:

The clipper circuits clips off the some part of the waveform depend on the applied reference voltage. Clipping circuits do not require energy storage elements these circuits can also used as sine to square wave converter at low amplitude signals.

QUESTION & ANSWERS:

1. In the fig.1 if reference voltage is 0v then what will be the output?

Ans. If the reference voltage is 0v,then the whole positive peak is clipped off and only the negative peak is appeared at the output.

2. What are the other names for the clippers?

Ans. Clippers are also called as amplitude limiters, slicers, voltage limiters.

EXPERIMENT NO-2(B)

NON LINEAR WAVE SHAPPING-CLAMPERS

AIM:

To verify the output of different diode clamping circuits.

APPARATUS REQUIRED:

Name of the Component/Equipment	Specifications	Quantity
Resistors	10KΩ	1
Capacitor	100uF, 100pF	1
Diode	1N4007	1
CRO	20MHz	1
Function generator	1MHz	1

THEORY:

The circuits which are used to add a d.c level as per the requirement to the a.c signals are called clamper circuits. Capacitor, diode, resistor are the three basic elements of a clamper circuit. The clamper circuits are also called d.c restorer or d.c inserter circuits. The clampers are classified as

1. Negative clampers
2. Positive clampers

CIRCUIT DIAGRAMS

POSITIVE PEAK CLAMPING TO 0V:

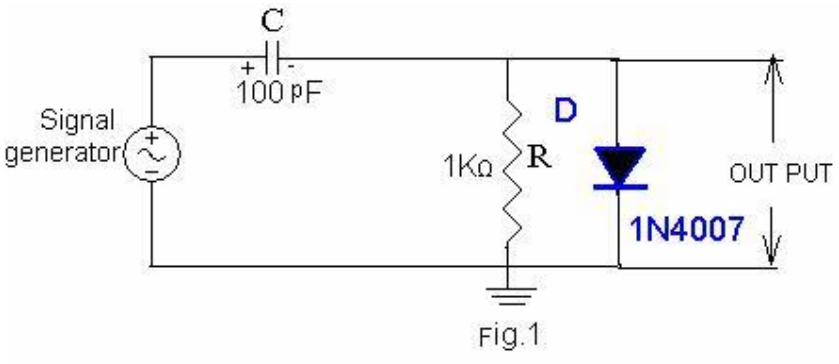


Fig.1

POSITIVE PEAK CLAMPING TO V_R=2V

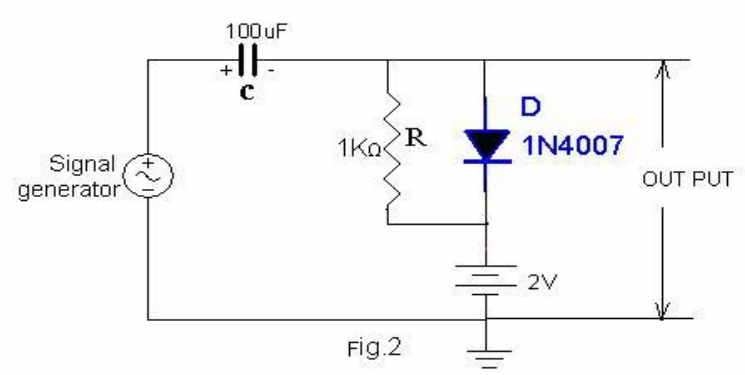


Fig.2

NEGATIVE PEAK CLAMPING TO V_R=0V

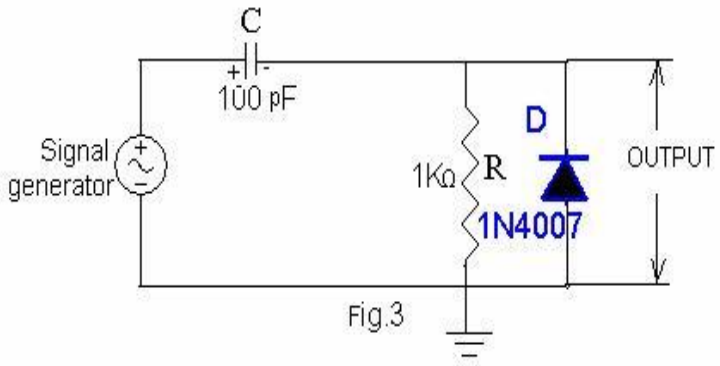


Fig.3

NEGATIVE PEAK CLAMPING TO V_R= -2V

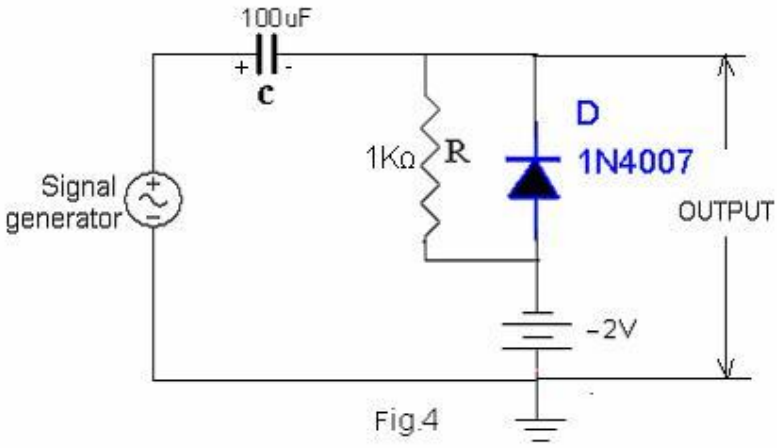


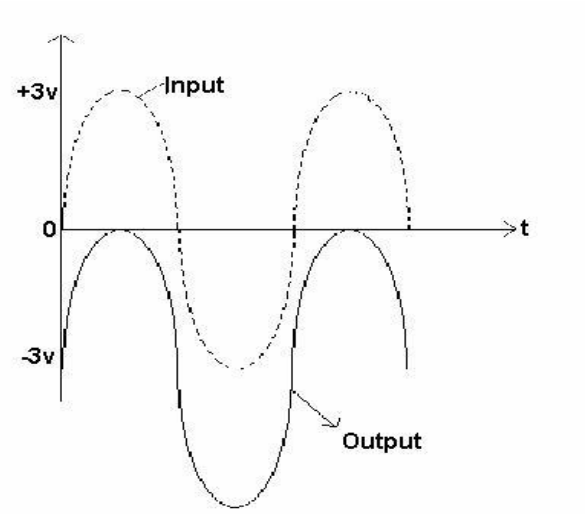
Fig.4

PROCEDURE:

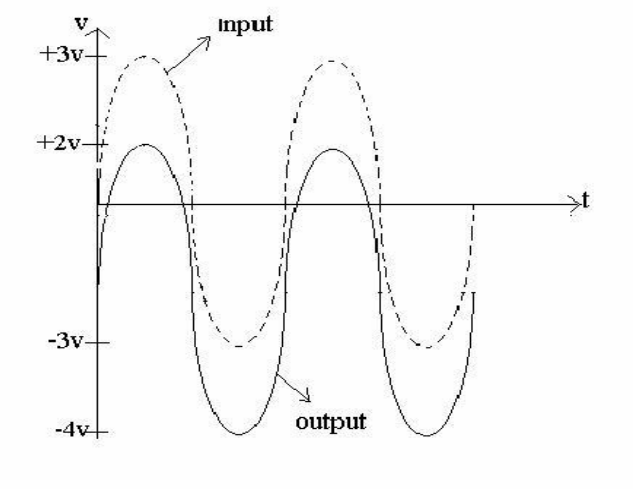
1. Connect the circuit as per circuit diagram.
2. Obtain a constant amplitude sine wave from function generator of 6 Vp-p, frequency of 1 KHz and give the signal as input to the circuit.
3. Observe and draw the output waveform and note down the amplitude at which clamping occurs.
4. Repeat the steps 1 to 3 for all circuits.

MODEL WAVEFORMS:

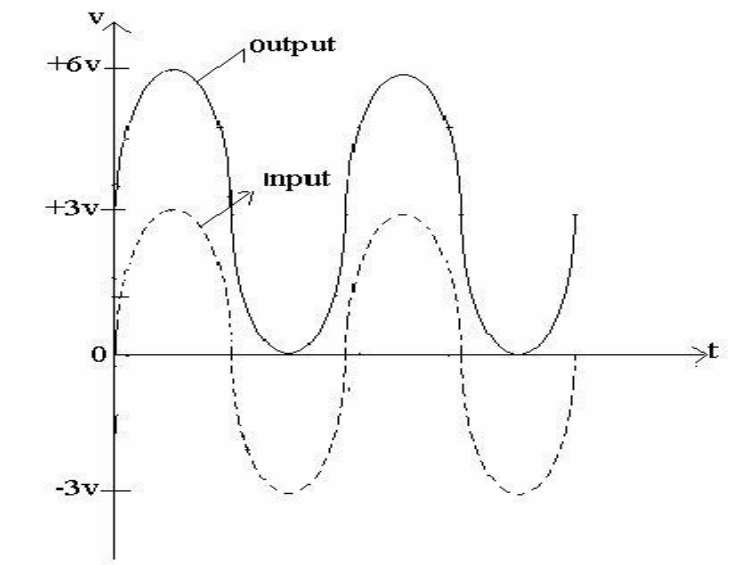
POSITIVE PEAK CLAMPING TO 0V:



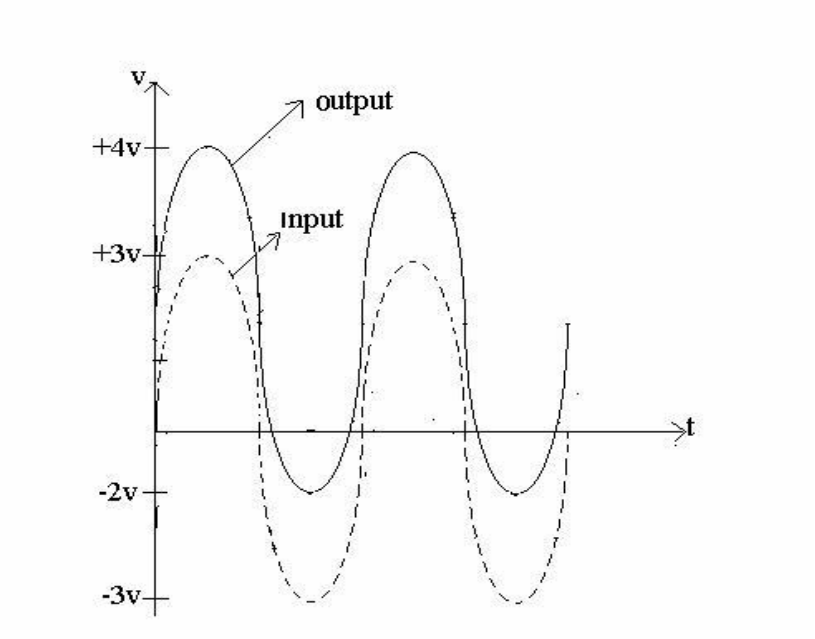
POSITIVE PEAK CLAMPING TO V_R=2V



NEGATIVE PEAK CLAMPING TO 0V



NEGATIVE PEAK CLAMPING TO VR= -2V



PRECAUTIONS:

1. Connections should be made carefully.
2. Verify the circuit before giving supply.
3. Take readings without any parallax error.

RESULT:

Different clamping circuits are constructed and their performance is observed.

INFERENCE:

In positive peak clamping, Positive peak of the sinusoidal waveform is clamped to 0v when reference voltage is 0v, and clamped to 2v when reference voltage is 2v.That is the waveform is shifted to negative side. So we called this clamper as negative clamper. In negative peak clamping, negative peak of the sinusoidal waveform is clamped to 0v when reference voltage is 0v, and clamped to -2v when reference voltage is -2v.That is the waveform is shifted to positive side. So we called this clamper as positive clamper.

QUESTION & ANSWERS

1. What is a clamper?

Ans. Clamping circuits are circuits, which are used to clamp or fix the extremity of a periodic wave form to some constant reference level .

2. Give some practical applications of clamper.

Ans. Horizontal section in TV to separate the sync signals, Voltage doubler circuits.

3. What is the purpose of shunt resistance in clamper?

Ans. If the amplitude of the input signal is decreased after the study state condition has been reached, there is no path for the capacitor to discharge. To permit the voltage across the capacitor to discharge. It is necessary to shunt a resistor across C, or equivalently to shunt a resistor across diode.

EXPERIMENT NO-3

TRANSISTOR AS A SWITCH

AIM:

To obtain characteristics of a transistor as a switch.

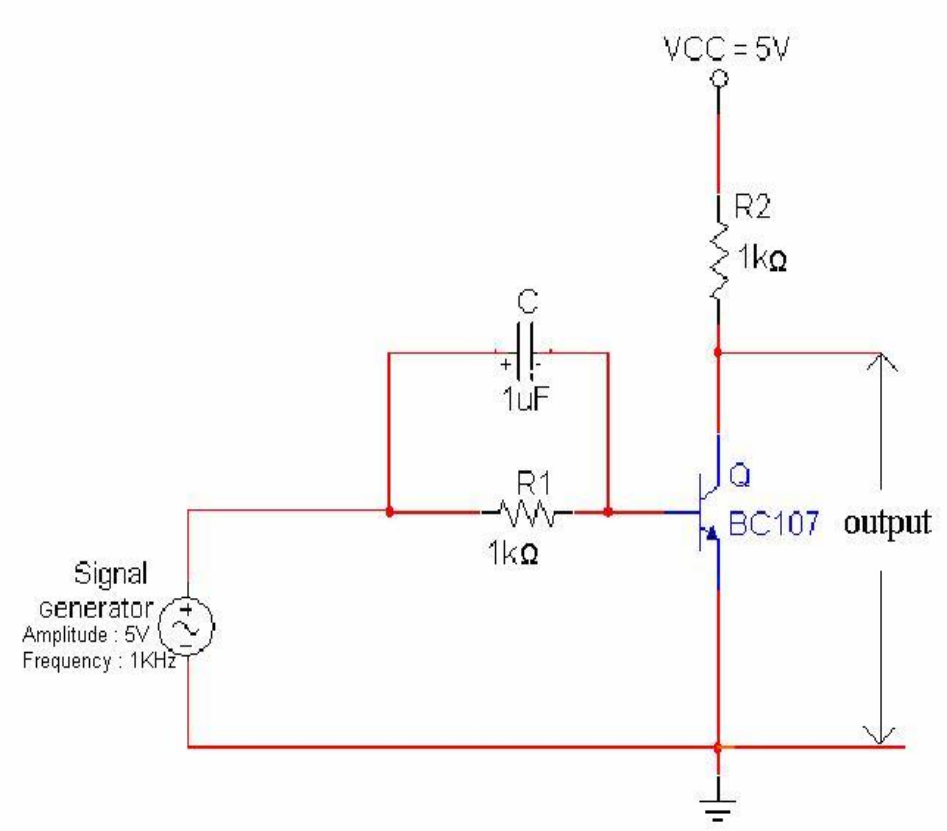
APPARATUS REQUIRED:

Name of the Component/Equipment	Specifications	Quantity
Transistor	BC 107	1
Diode	0A79	1
Resistors	10K	2
	5.6KΩ	2
Capacitor	100pF	1
CRO	20MHz(BW)	1
Function generator	1MHz	1
Regulated Power Supply	0-30V, 1A	1

THEORY:

Transistors are widely used in digital logic circuits and switching applications. In these applications the voltage levels periodically alternate between a "LOW" and a "HIGH" voltage, such as 0V and +5V. In switching circuits, a transistor is operated at cutoff for the OFF condition, and in saturation for the ON condition. The active linear region is passed through abruptly switching from cutoff to saturation or vice versa. In cutoff region, both the transistor junctions between Emitter and Base and the junction between Base and Collector are reverse biased and only the reverse current which is very small and practically neglected, flows in the transistor. In saturation region both junctions are in forward bias and the values of V_{ce}(sat) and V_{be}(sat) are small.

CIRCUIT DIAGRAM:



PROCEDURE:

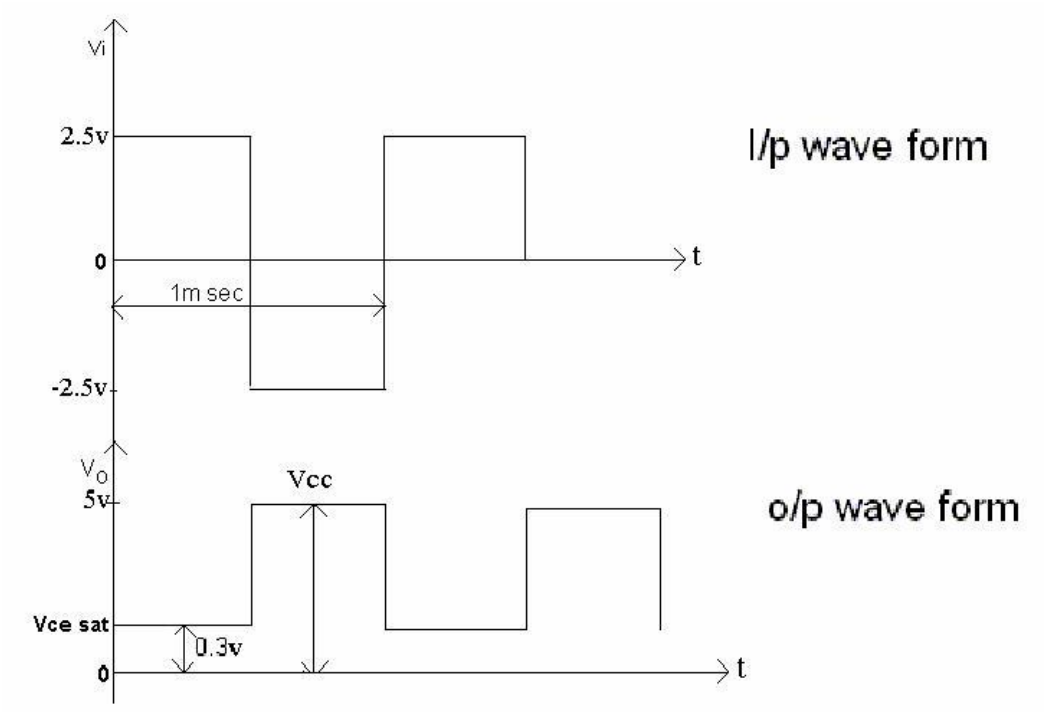
1. Connect the circuit as per circuit diagram.

2. Obtain a constant amplitude square wave from function generator of 5V p-p and give the signal as input to the circuit.

3. Observe the output waveform and note down its voltage amplitude levels.

4. Draw the input and output waveforms

Model graph:



THEORETICAL CALICULATIONS:

When Vi= +2.5v, the transistor goes into saturation region.
So $V_{O=}V_{ce\ sat=}0.3V$.
When V_i=-2.5v, the transistor is in cutoff region so V_o=Vcc=5v

PRECAUTIONS:

1. Connections should be made carefully.
2. Verify the circuit before giving supply voltage.
3. Take readings without any parallax error.

RESULT:

Switching characteristics of a transistor are observed.

INFERENCE:

When both collector and emitter junctions of a transistor are reversed biased transistor is in cutoff state and it acts as a open switch. When emitter junction forward biased but collector junction is reversed biased , the transistor operates in the active region and it act as an amplifier. When the both the emitter and collector junctions are forward biased the transistor in saturation and it acts as closed switch.

QUESTION & ANSWERS:

1. What are the limitations of transistor switch?

Ans. Switching speed is low; collector to emitter saturation voltage is higher than the FET saturation voltage.

2. What is the turn on time of a transistor?

Ans. When the voltage pulse is applied to the transistor, the sum of the time required for the collector to change from zero to 10 percent of the maximum current (delay time), and time required to rise from 10 to 90 percent of its saturation value (rise time) is called turn-on time of a transistor.

EXPERIMENT NO-4

BISTABLE MULTIVIBRATOR

Aim:

To Observe the stable states voltages of Bistable Multivibrator.

Apparatus required:

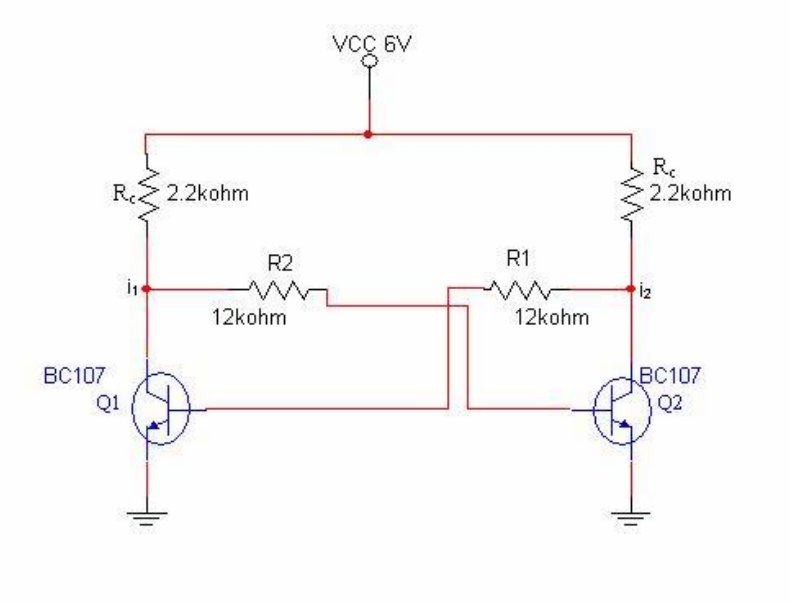
Name of the Component/Equipment	Specifications	Quantity
Transistor	BC 107	2
Resistors	2.2KΩ	2
	12KΩ	2
Regulated Power Supply	0-30V, 1A	1

THEORY:

The circuit diagram of a fixed bias bistable multivibrator using transistors. The output of each amplifier is direct coupled to the input of the other amplifier. In one of the stable states transistor Q_1 and Q_2 is off and in the other stable state. Q_1 is off and Q_2 is on even though the circuit is symmetrical; it is not possible for the circuit to remain in a stable state with both the transistors conducting simultaneously and caring equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents i_1 and i_2 suppose there is a minute fluctuation in the current i_1-let us say it increases by a small amount.

Then the voltage at the collector of q_1 decreases. This will result in a decrease in voltage at the base of q_2. So q_2 conducts less and i_2 decreases and hence the potential at the collector of q_2 increases. This results in an increase in the base potential of q1.So q_1 conducts still more and i_1 is further increased and the potential at the collector of q_1 is further decreased, and so on . So the current i_1 keeps on increasing and the current i_2 keeps on decreasing till q_1 goes in to saturation and q_2 goes in to cut-off. This action takes place because of the regenerative feed –back incorporated into the circuit and will occur only if the loop gain is greater than one.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in figure.

2. Verify the stable state by measuring the voltages at two collectors by using multimeter.

3. Note down the corresponding base voltages of the same state (say state-1).

4. To change the state, apply negative voltage (say-2v) to the base of on transistor or positive voltage to the base of transistor (through proper current limiting resistance).

5. Verify the state by measuring voltages at collector and also note down voltages at each base.

OBSERVATIONS :

Sample Readings

Before Triggering

Q_1(OFF)	Q_1(ON)
V_{BE1}=0.03V	V_{BE2}=0.65V
V_{CE1}=5.6V	V_{CE2}=0.03V

After Triggering

Q_1(ON)	Q_1(OFF)
V_{BE1}=0.65V	V_{BE2}=0.01V
V_{CE1}=0.03V	V_{CE2}=5.6V

PRECAUTIONS:

1. Connections should be made carefully.
2. Note down the parameters carefully.
3. The supply voltage levels should not exceed the maximum rating of the transistor.

INFERENCE:

The bistable circuit can exist in definitely in either of two stable states and which can be induced to make an abrupt transsion from one state to other by means of external excitation. So it can be used as memory element which can store one bit of data.

RESULT: The stable state voltages of a bistable multivibrator are observed.

QUESTION & ANSWERS:

1. What do you mean by a bistable circuit?

Ans. A bistable circuit is one which can exist indefinitely in either of two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation.

2. What are the other names of a bistable multivibrator?

Ans. Ecless Jordan circuit, Trigger circuit, Scale-of-2, Toggle circuit, Flip flop, Binary.

3. What do you mean by triggering signal?

Ans. The triggering signal is employed to induce a transition from one state to other is either a pulse of short duration of step voltage.

EXPERIMENT NO-5

MONOSTABLE MULTIVIBRATOR

AIM:

To observe the stable state and quasi stable state voltages in monostable multivibrator.

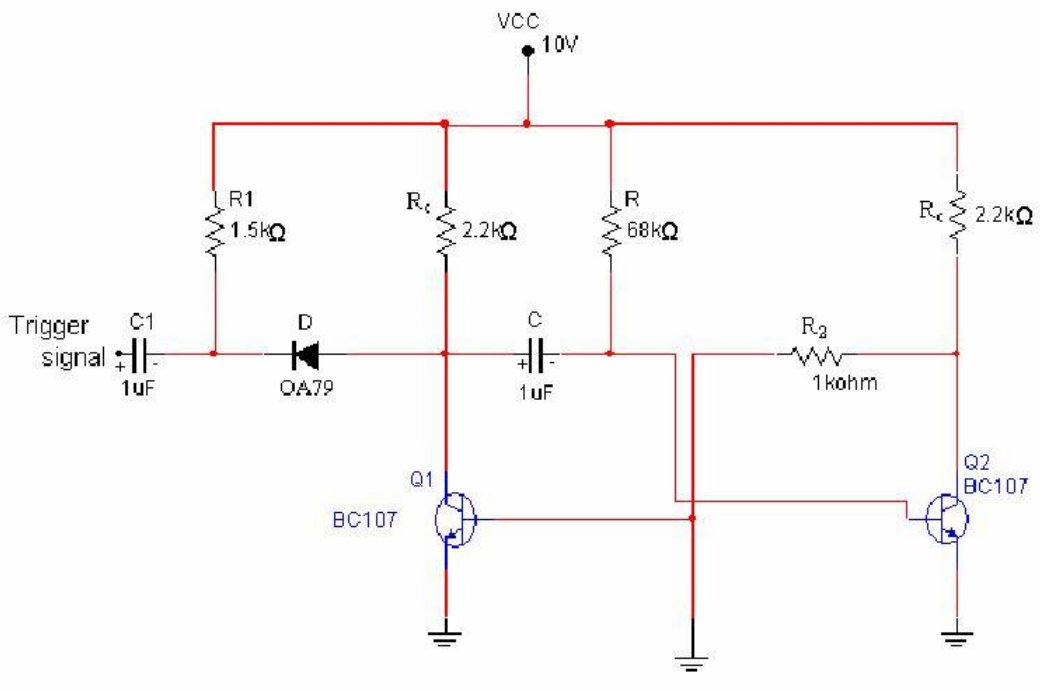
APPARATUS REQUIRED:

Name of the Component/Equipment	Specifications	Quantity
Transistor (BC 107)		2
Resistors	1.5KΩ	1
	2.2KΩ	2
	68KΩ	1
	1KΩ	1
Capacitor	1μF	2
Diode	0A79	1
CRO	20MHz	1
Function generator	1MHz	1
Regulated Power Supply	0-30V, 1A	1

THEORY:

A monostable multivibrator on the other hand compared to astable, bistable has only one stable state, the other state being quasi stable state. Normally the multivibrator is in stable state and when an externally triggering pulse is applied, it switches from the stable to the quasi stable state. It remains in the quasi stable state for a short duration, but automatically reverse switches back to its origional stable state without any triggering pulse.The monostable multivibrator is also referred as ‘one shot’ or ‘uni vibrator’ since only one triggering signal is required to reverse the original stable state. The duration of quasi stable state is termed as delay time (or) pulse width (or) gate time.It is denoted as ‘t’.

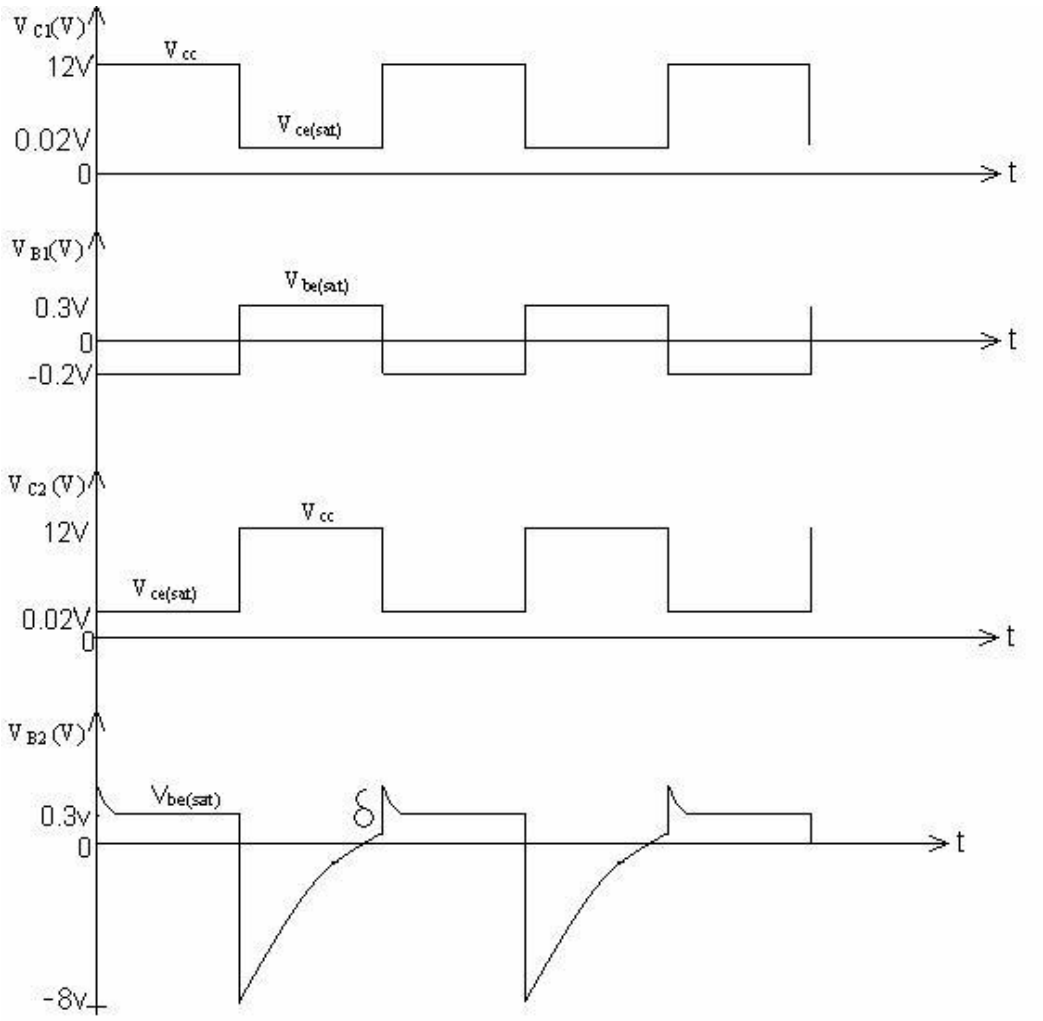
CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Verify the stable states of Q_1 and Q_2
3. Apply the square wave of 2v p-p , 1KHz signal to the trigger circuit.
4 Observe the wave forms at base of each transistor simultaneously.
5. Observe the wave forms at collectors of each transistors simultaneously.
6.. Note down the parameters carefully.
7 Note down the time period and compare it with theoretical values.
8. Plot wave forms of V_{b1}, V_{b2},V_{c1} & V_{c2} with respect to time .

MODEL WAVEFORMS:



CALCULATIONS:

Theoretical Values:

Time Period, T = 0.693RC

$= 0.693 \times 68 \times 10^{3} \times 0.01 \times 10^{-6}$

= 47μ sec

= 0.047 m sec

Frequency, f = 1/T = 21 kHz

PRECAUTIONS:

1. Connections should be made carefully.
2. Note down the parameters without parallax error.
3. The supply voltage levels should not exceed the maximum rating of the transistor.

INFERENCE:

The output of the monostable multivibrator while it remains in the quasi stable state is a pulse of duration t_1 whose value depends up on the circuit components. Hence monostable multivibrator is called as a pulse generator.

RESULT:

Stable state and quasi stable state voltages in monostable multivibrator are observed

.

QUESTION & ANSWERS:

1. What are the other names of Mono Stable multivibrator ?

Ans.Uni vibrator, Gating circuit, Delay circuit, One shot.

2. Which type of triggering is used in mono stable multi vibrator ?

Ans. Unsymetrical Triggering is used in mono stable multi vibrator

3. Define transition time?

Ans. The time interval during which conduction transfers from one transistor to another is called transition time.

EXPERIMENT NO-6

ASTABLE MULTIVIBRATOR

AIM:

To Observe the ON & OFF states of Transistor in an Astable Multivibrator.

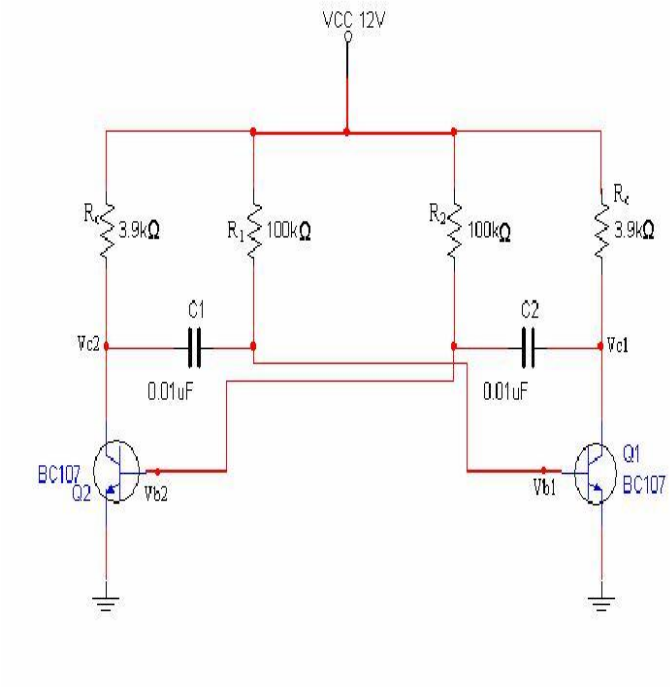
APPARATUS REQUIRED:

Name of the Component/Equipment	Specifications	Quantity
Transistor (BC 107)	BC 107	2
Resistors	3.9KΩ	2
	100KΩ	2
Capacitor	0.01μF	2
Regulated Power Supply	0-30V, 1A	1

THEORY :

An Astable Multivibrator has two quasi stable states and it keeps on switching between these two states by itself . No external triggering signal is needed. The astable multivibrator cannot remain indefinitely in any one of the two states .The two amplifier stages of an astable multivibrator are regenerative across coupled by capacitors. The astable multivibrator may be to generate a square wave of period, 1.38RC

CIRCUIT DIAGRAM



PROCEDURE :

1. Calculate the theoratical frequency of oscillations of the circuit.

2.Connect the circuit as per the circuit diagram.

3 Observe the voltage wave forms at both collectors of two transistors simultaneously.

4. Observe the voltage wave forms at each base simultaneously with corresponding collector voltage.

5. Note down the values of wave forms carefully.

6. Compare the theoratical and practical values.

CALCULATIONS:

THEORITICAL VALUES :

$RC = R_1C_1 + R_2C_2$

Time Period, $T = 1.368RC$

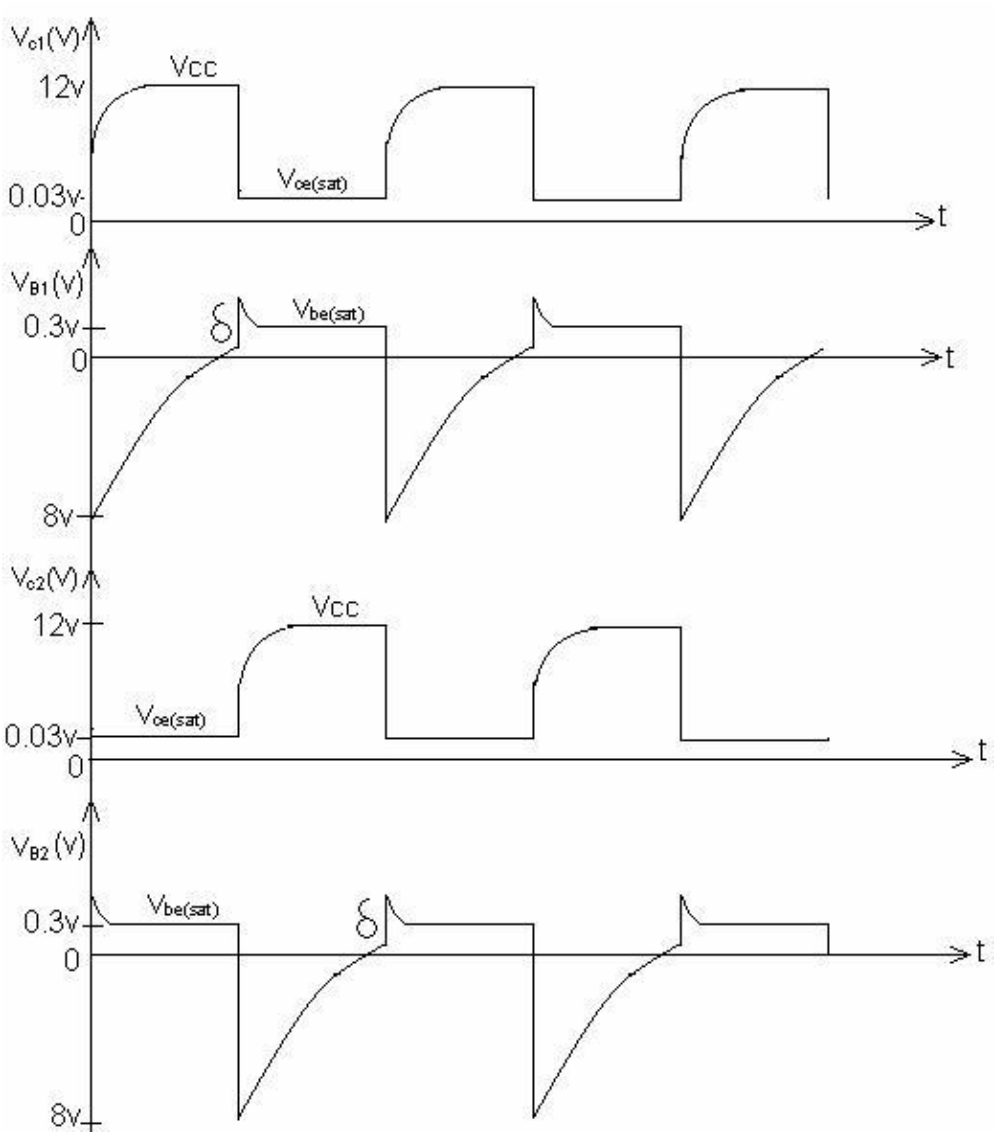
$= 1.368 \times 100 \times 10^{3} \times 0.01 \times 10^{-6}$

$= 93\ \mu$ sec

$= 0.093$ m sec

Frequency, $f = 1/T = 10.75$kHz

MODEL WAVEFORMS :



PRECAUTIONS :

1. Connections should be made carefully.
2. Readings should be noted without parallax error**.**

RESULT :

The wave forms of astable multivibrator has been verified.

INFERENCE :

The astable circuit has two states, both of which are quasi stable states.

QUESTION & ANSWERS :

1.Define stable state ?

Ans Stable state of a binary is one in which the voltages and currents satisfy the kirchhoff's laws and are consistent with the device cheracteristics and in which,in addition, the condition of the loop gain being less than unity is satisfied.

2.Define quasi stable state ?

Ans It is temporary state , after predefined time circuit comes to steady state.

EXPERIMENT NO-7

UJT RELAXATION OSCILLATOR

AIM:

To obtain the characteristics of UJT Relaxation Oscillator.

APPARATUS REQUIRED:

Name of the Component/Equipment	Specifications	Quantity
UJT	2N 2646	1
Resistors	220Ω	1
	68KΩ	1
	120Ω	1
Capacitor	0.1μF	1
	0.01μF	1
	0.001μF	1
Diode	0A79	1
Inductor	130mH	1
CRO	20MHz	1
Function generator	1MHz	1
Regulated Power Supply	(0-30V),1A	1

THEORY:

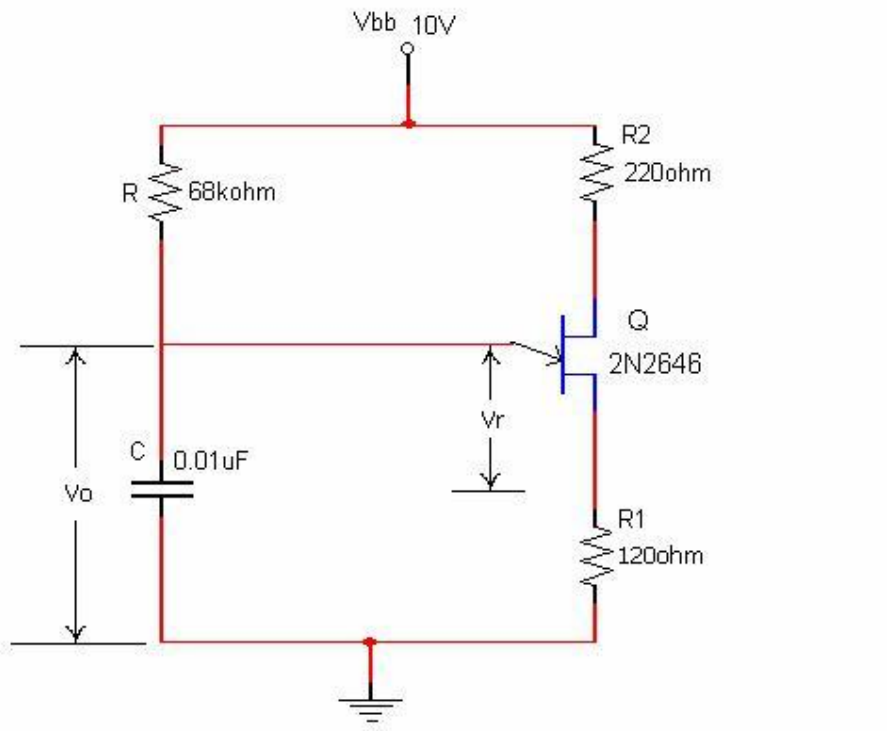
Many devices such as transistor,UJT, FET can be used as a switch. Here UJT is used as a switch to obtain the sweep voltage. Capacitor C charges through the resistor,R towards supply Voltage,V_{bb}. As long as the capacitor voltage is less than peak Voltage,V_p, the emitter appears as an open circuit.

$V_p = \eta V_{bb} + V_\gamma$ where = stand off ratio of UJT,

V_γ = Cut in voltage of diode.

When the voltage V_o exceeds voltage V_p, the UJT fires. The Capacitor starts discharging through $R_1 + R_{b1}$. Where, R_{b1} is the internal base resistance. This process is repeated until the power supply is available.

CIRCUIT DIAGRAM:



DESIGN EQUATIONS:

THEORETICAL CALCULATIONS:

$V_p = V_\gamma + (R_1 / R_1 R_2) V_{bb}$

$= 0.7 + (120/120+220)10$

$= 8.57V$

1. When C=0.1μF

$T_c = RC \ln(V_{bb} - V_v / V_{bb} - V_p) = (68K)(0.1\mu F)(12/12-8.57)$

$= 3.6ms$

$T_d = R_1C = (120)(0.1\mu) = 12\ \mu sec.$

2. When C=0.01μF

$T_c = RC \ln(V_{bb} - V_v / V_{bb} - V_p)$

$= (68K)(0.01\mu F)(12/12-8.5)$

$= 365\mu s$

$T_d = R_1C = (120)(0.01\mu) = 1.2\ \mu sec.$

3. When C=0.001µF

$T_c = RC \ln(V_{bb} - V_v / V_{bb} - V_p)$

$=(68K)\ (0.001\mu F)\ (12/12-8.5)$

$= 36.5\mu s$

$T_d = R_1C = (120)(0.01\mu) = 0.12\ \mu sec$

S.NO	Capacitance value (µF)	Theoretical time period	Practical time period
1	0.1	3.65 ms	3.6 ms
2	0.01	0.365 ms	0.32 ms
3	0.001	36.58µs	40µs

PROCEDURE:

1) Connect the circuit as shown in figA.

2) Observe the voltage waveform across the capacitor, C.

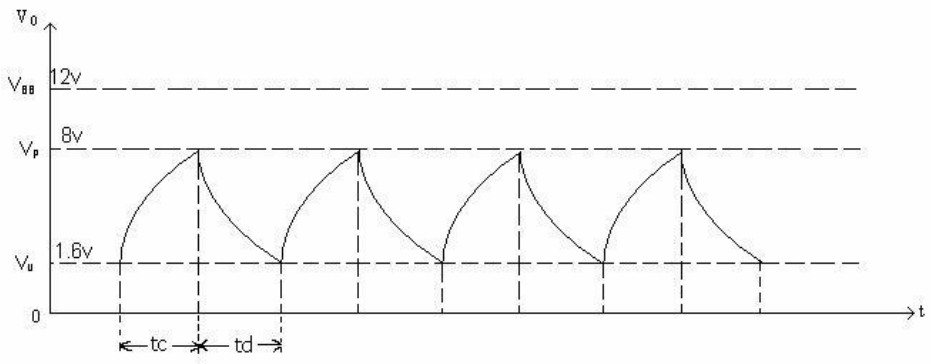
3) Change the time constant by changing the capacitor values to 0.1µF and 0.001 µF and observe the wave forms.

4) Note down the parameters, amplitude, charging and discharging periods of the wave forms

5)Compare the theoretical and practical time periods.

6)Plot the graph between voltage across capacitor with respect to time

MODEL GRAPH:



PRECAUTIONS:

1.Connections should be given carefully.

2. Readings should be noted without parallox error.

RESULT:

Performance and construction of UJT Relaxation Oscillator is observed.

INFERENCE:

Two separate power supplies one for active component and the other for linear network must be used in order to increase the linearity of the waveform.

QUESTION & ANSWERS :

1.What do you mean by a) voltage time base generator, b) a current time base Generator.

Ans: Voltage time base generator: The electronic circuit which generates an output voltagethat varies linearly with time.

Current time base generator: The electronic circuit which generates output current that varies linearly with time.

2.What are the applications of time base generator?

Ans:CRO's,Radar,television,time modulation,precise time measurements

3.What are the methods of generating a time base waveform?

Ans:Exponential charging,Constant current charging,Miller circuit,Bootstrcircuit,compensating circuits.

EXPERIMENT NO-8

SCHMITT TRIGGER

AIM:

To Generate a square wave from a given sine wave using Schmitt Trigger

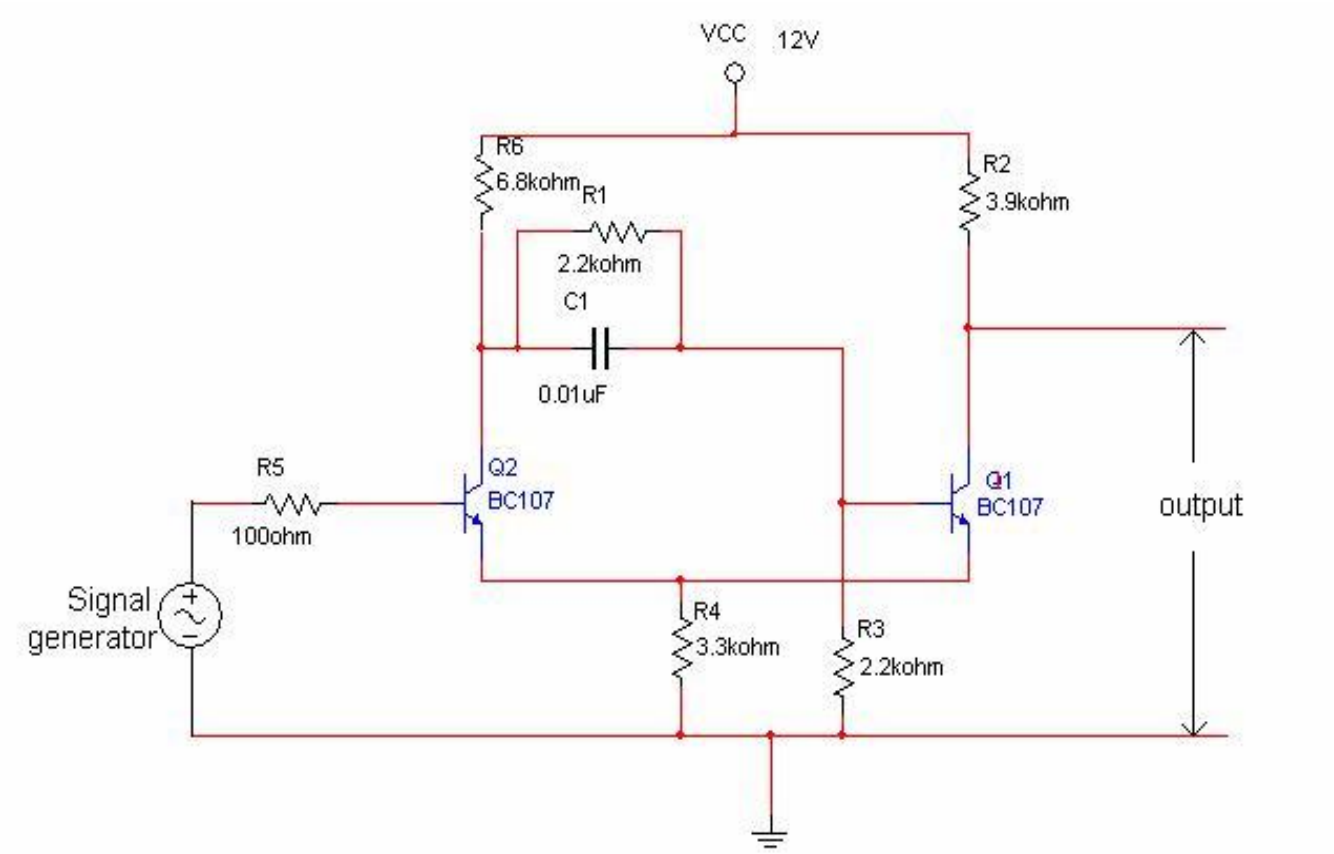
APPARATUS REQUIRED:

Name of the Component/Equipment	Values/Specifications	Quantity
Transistor	BC 107	2
Resistors	100Ω	1
	6.8KΩ	1
	3.9KΩ	1
	2.7KΩ	1
	2.2KΩ	1
Capacitor	0.01µF	1
CRO	20MHz	1
Regulated Power Supply	30V	1
Function generator	1MHz	1

THEORY:

Schmitt trigger is a bistable circuit and the existence of only two stable states results form the fact that positive feedback is incorporated into the circuit and from the further fact that the loop gain of the circuit is greater than unity. There are several ways to adjust the loop gain. One way of adjusting the loop gain is by varying Rc1. Under quiescent conditions Q1 is OFF and Q2 is ON because it gets the required base drive from Vcc through Rc1 and R1. So the output voltage is Vo=Vcc-Ic2Rc2 is at its lower level. Untill then the output remains at its lower level.

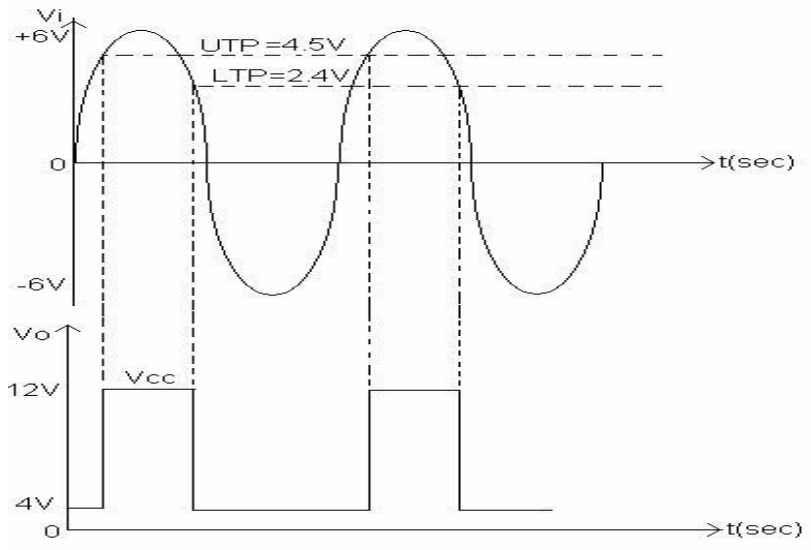
CIRCUIT DIAGRAM :



PROCEDURE:

1. Connect the circuit as per circuit diagram.
2. Apply a sine wave of peak to peak amplitude 10V, 1 KHz frequency wave as input to the circuit.
3. Observe input and output waveforms simultaneously in channel 1 and channel 2 of CRO.
4. Note down the input voltage levels at which output changes the voltage level.
5. Draw the graph between voltage versus time of input and output signals.

MODEL GRAPH:



PRECAUTIONS:

1. Connections should be made carefully.
2. Readings should be noted carefully without any parallax error.

RESULT: Schmitt trigger is constructed and observed its performance.

INFERENCE:

Schmitt trigger circuit is a emitter coupled bistable circuit, and existence of only two stable states results from the fact that positive feedback is incorporated into the circuit, and from the further fact that the loop gain of the circuit is greater than unity.

QUESTION & ANSWERS:

1. What is the other name of the Schmitt trigger?

Ans Emitter coupled Binary

2. What are the applications of the Schmitt trigger?

Ans Amplitude Comparator, Squaring circuit

3. Define the terms UTP & LTP?

Ans. UTP is defined as the input voltage at which Q1 starts conducting, LTP is defined as the input voltage at which Q2 resumes conduction.

EXPERIMENT NO-9

BOOT STRAP SWEEP CIRCUIT

AIM:

To observe the characteristics of a boot strap sweep circuit.

APPARATUS REQUIRED:

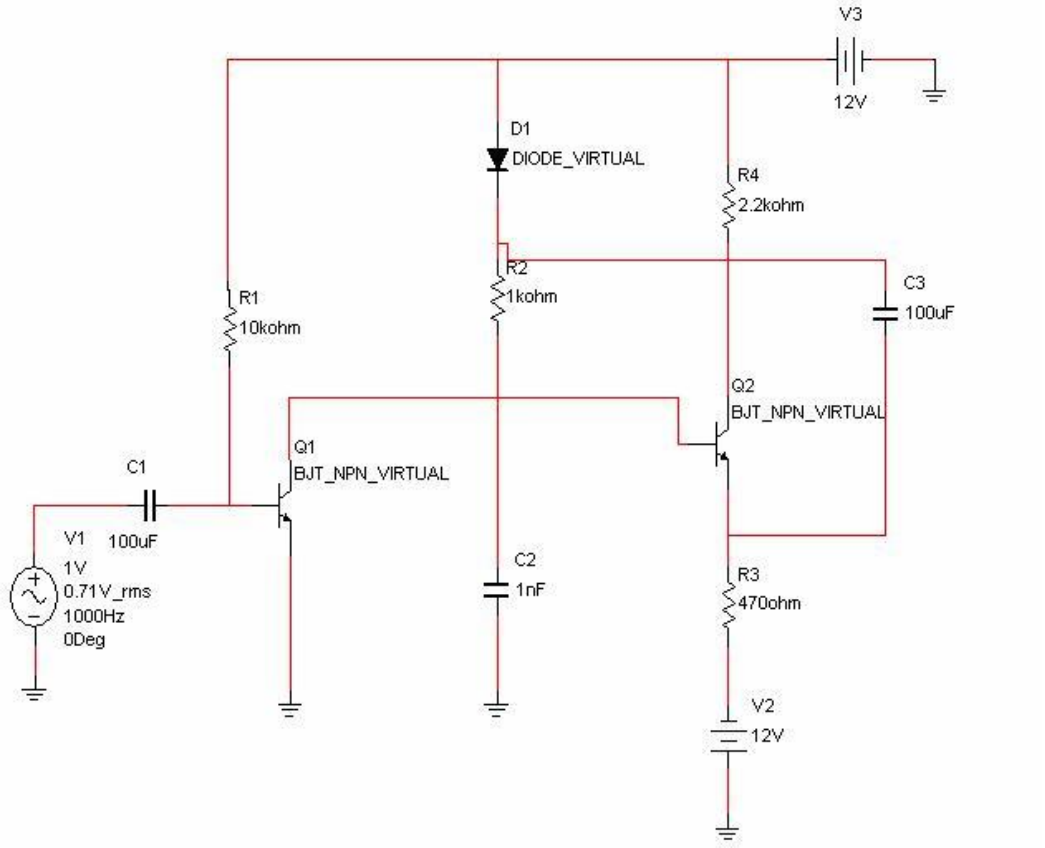
Name of the Component/Equipment	Specifications	Quantity
Transistor	BC 107	2
Resistors	220Ω	1
	1KΩ	1
	470 Ω	1
	10Ω	1
Capacitor	100µF	2
	1µF	1
	0.001µF	1
Diode	2N2222	1
CRO	20MHz	1
Function generator	1MHz	1
Regulated Power Supply	(0-30V),1A	1

THEORY:

Boot strap sweep generator is a technique used to generate a sweep with relatively less slope error when compared to the exponential sweep. This is achieved by maintaining a constant current through a resistor,by maintaing a constant voltage across it In the circuit shown Q1 acts as a switch which should be opened to initiate the sweep.Voltage across resistor is maintained constant (Vce) hence a constant current (Vcc/r) will charge the capacitor C.Transistor Q2 will act as an amplifier with high input impedance and

voltage gain '1' (emitter follower) .Hence the same sweep which is generated across C will also appear at the output

CIRCUIT DIAGRAM:



DESIGN EQUATIONS:

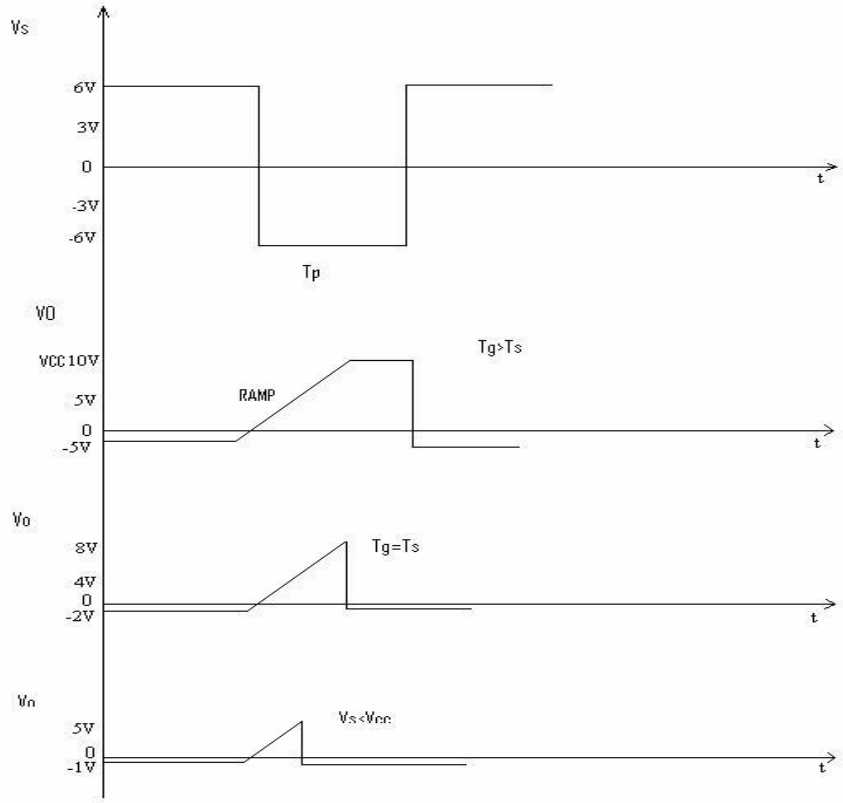
$T_S(max)=RC$

Assume 'C' and find 'R' for given maximum sweep
Select R_b to provide enough bias for switching transistor Q1

PROCEDURE:

1. Connect the circuit as shown in the figure.
2. Apply the square wave input to the circuit (which is generated in the module itself).
3. Observe the output wave form.
4. By varying the input frequency observe the variations in the output.
5. Note the maximum value of sweep and starting voltage.
6. Note the sweep time Ts.

WAVE FORMS:



RESULT :

The characteristics of Boot strap sweep circuit are observed.

INFERENCE:

The linearity of the voltage time base increases as gate width decreases.

QUESTION & ANSWERS :

1 .What are the other methods of sweep generator?

Ans:Exponential charging,Constant current charging, Miller sweep circuit, Comensating networks,Inductor circuits

2. Compare bootstrap and miller sweep generator?

Ans:a)The Bootstrap circuit employes positive feedback where as Miller sweep employes negative feedback

b) The Bootstrap circuit employes an emitter follower with unity voltage gain where as Miller sweep employes an amplifier with very large voltage gain.

EXPERIMENT NO-10.

STUDY OF LOGIC GATES

IM:

To construct the basic and universal gates using discrete components and

Verify truth table.

APPARATUS REQUIRED:

Name of the Component/Equipment	Specifications	Quantity
Transistor	BC 107	1
Diode	IN4007	1
Resistors	4.7KΩ	2
	100KΩ	1
LED	-	1
Bread Board	-	1
Regulated Power Supply	0-30V, 1A	1

THEORY:

1. OR-GATE:

OR gate has two or more inputs and a single output and it operates in accordance with the following definitions.The output of an OR gate is high if one or more inputs are high. When all the inputs are low then the output is low.If two or more inputs are in high state then the diodes connected to these inputs conduct and all other diodes remain reverse biased so the output will be high and OR function is satisfied.

2. AND-GATE:

AND gate has two or more inputs and a single output and it operates in accordance with the following definitions. The output of an AND gate is high if all inputs are high.

If V_r is chosen i.e. more positive than V_{cd} then all diodes will be conducting upon a coincidence and the output will be clamped at '1'.

If Vr is equal to V_{cd} then all diodes are cut-off and output will raise to the voltage V_r if not all inputs have same high value then the output of AND gate is equal to V_i (min0).

3. NOT-GATE:

The NOT gate circuit has a single output and a single input and perform the operation of negation in accordance with definition, the output of a NOT gate is high if the input is low and the output is low or zero if the input is high or 1.

4. NOR-GATE:

A negation following on OR is called as NOT-OR gate NOR gate. As shown in figure if Vo is applied as input signal to the diodes then both diodes are forward biased. Hence no voltage is applied to emitter base junction and total current is passed through the LED and it glows which indicates high or one state.

5. NAND-GATE:

The NAND gate can be implemented by placing a transistor NOT gate after the AND gate circuit with diodes. These gates are called diode-transistor logic gates.

If Vo is applied to input of the diode then the diode D1 and D2 will be forward biased. Hence no voltage applied across base-emitter junction and this junction goes into cut-off region. Hence total current from source Vce will flow through LED and it flows which indicate the one state or high state.

CIRCUIT DIAGRAMS:

1. OR GATE

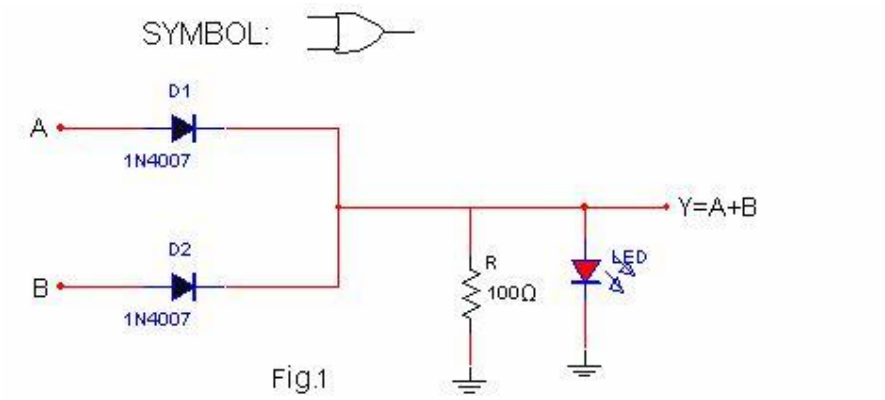


Fig.1

2.AND GATE

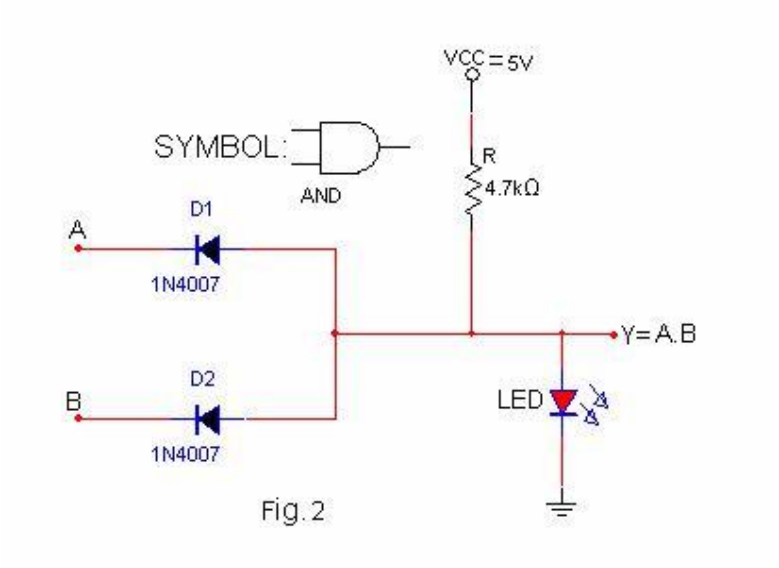


Fig. 2

3. NOT GATE:

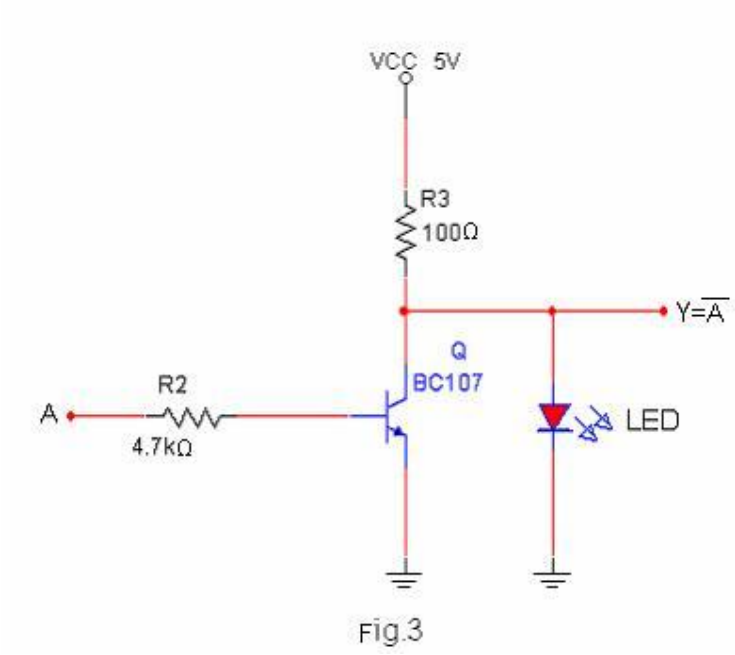


Fig.3

4. NOR GATE:

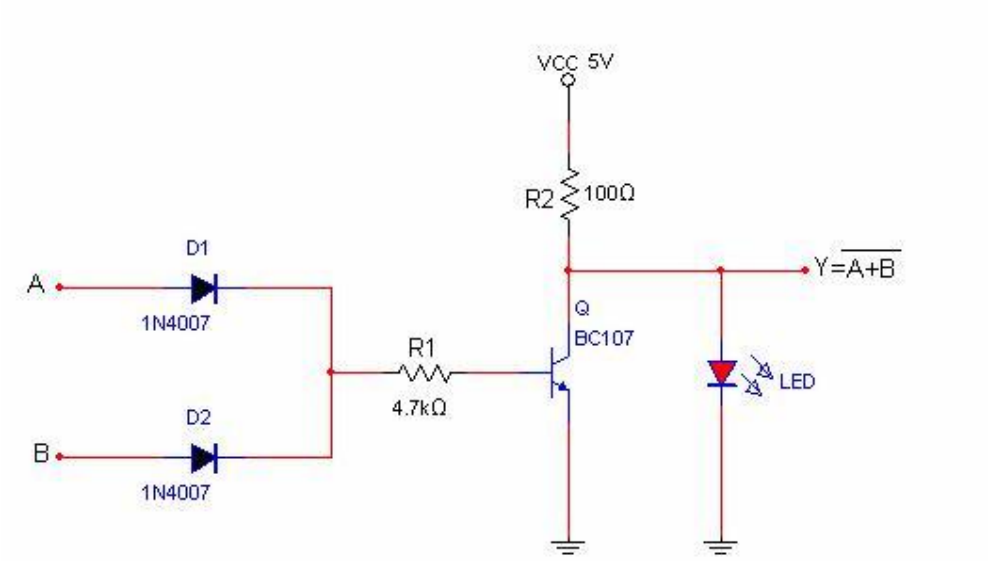


Fig.4

5. NAND GATE:

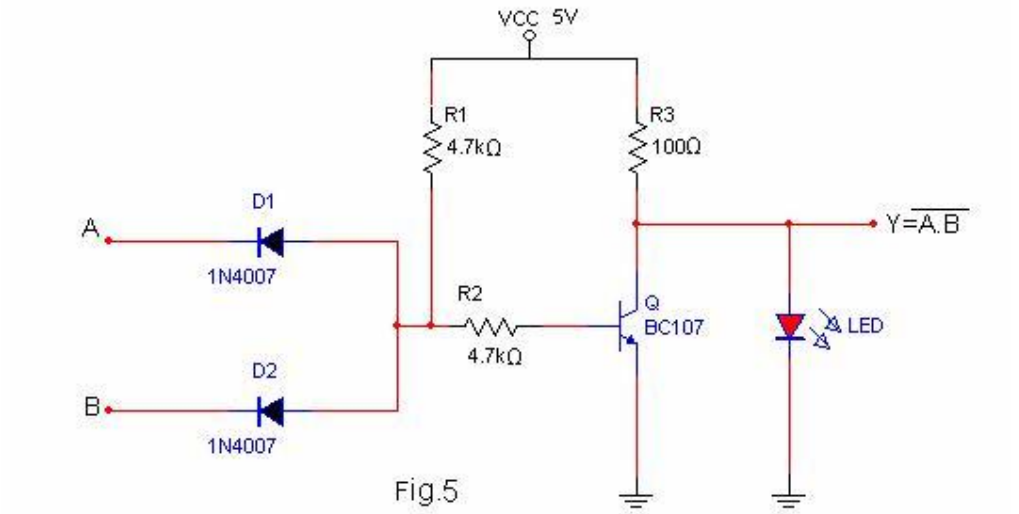


Fig.5

TRUTH TABLES:

1. AND GATE:

2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

2.OR GATE:

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT GATE:

NOT gate	
A	$\overline{A}$
0	1
1	0

4.NOR GATE

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

5. NAND GATE:

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

PROCEDURE:

1. Connect the circuit as per diagram.
2. Apply 5v from RPS for logic 1and 0v for logic 0.
3. Measure the output voltage using digital multimeter and verify the truth table.
4. Repeat the same for all circuits.
5.

RESULT:

Basic and universal gates are constructed using discrete components and their truth tables are verified.

INFERENCE:

Even in a large scale digital system, such as computer there are only a few basic operations which must be performed these operations, to be sure ,may be repeated very many times. The four circuits most commonly employed in such systems are known as the OR, AND, NOT and FLIP FLOP.

QUESTION & ANSWERS :

1. What are the universal gates? Why they are called universal gates?

Ans NAND and NOR gates are called universal gates, because using these two gates we can realize all other logic gates.

2. What is the other name of the EX-NOR gate?

Ans. Equalence Gate

EXPERIMENT NO-11

SAMPLING GATES

AIM:

To observe the output of a bidirectional sampling gate for given input of a sine wave with a gating signal of square wave.

APPARATUS REQUIRED:

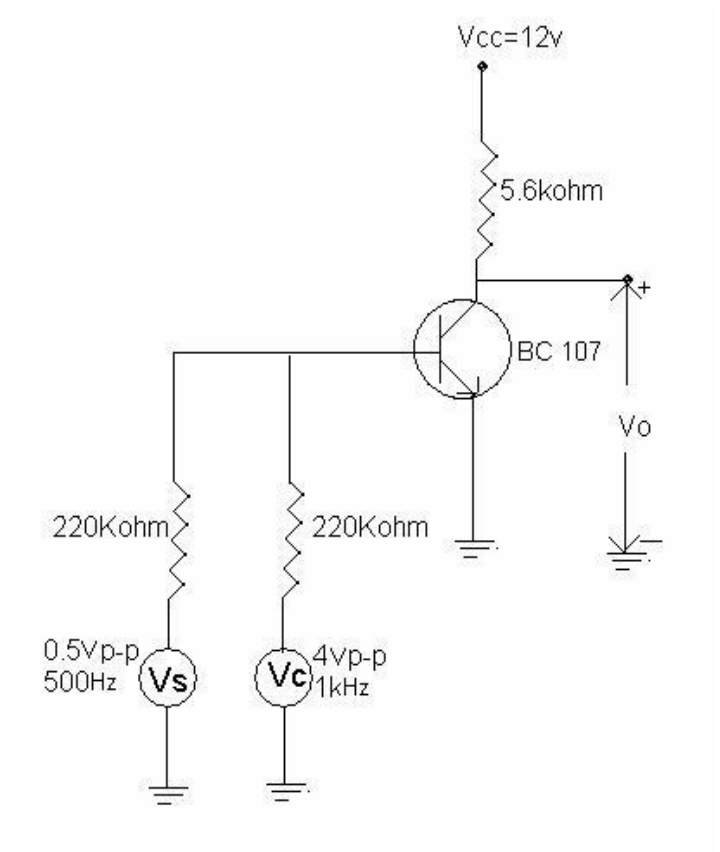
Name of the Component/Equipment	Specifications	Quantity
Transistor (BC 107)	-	1
Resistors	220KΩ	1
	5.6Ω	1
CRO	20MHz	1
Function generator	1MHz	2
Regulated Power Supply	0-30V, 1A	1

THEORY:

Sampling gate is a transmission network which transmits input wave form in a particular interval of time only, and for remaining time output is zero. There are two types of sampling gates. 1. Unidirectional sampling gates 2. Bidirectional sampling gates.

Unidirectional sampling gates are those which transmit signals of only one polarity. Bidirectional sampling gates are those which transmit signals of both polarities When gating signal is at it's lower level transistor is well cutoff and output is Vcc. When gating signal is at its higher level transistor goes into active region so input signal is sampled and appears at output.

CIRCUIT DIAGRAM:



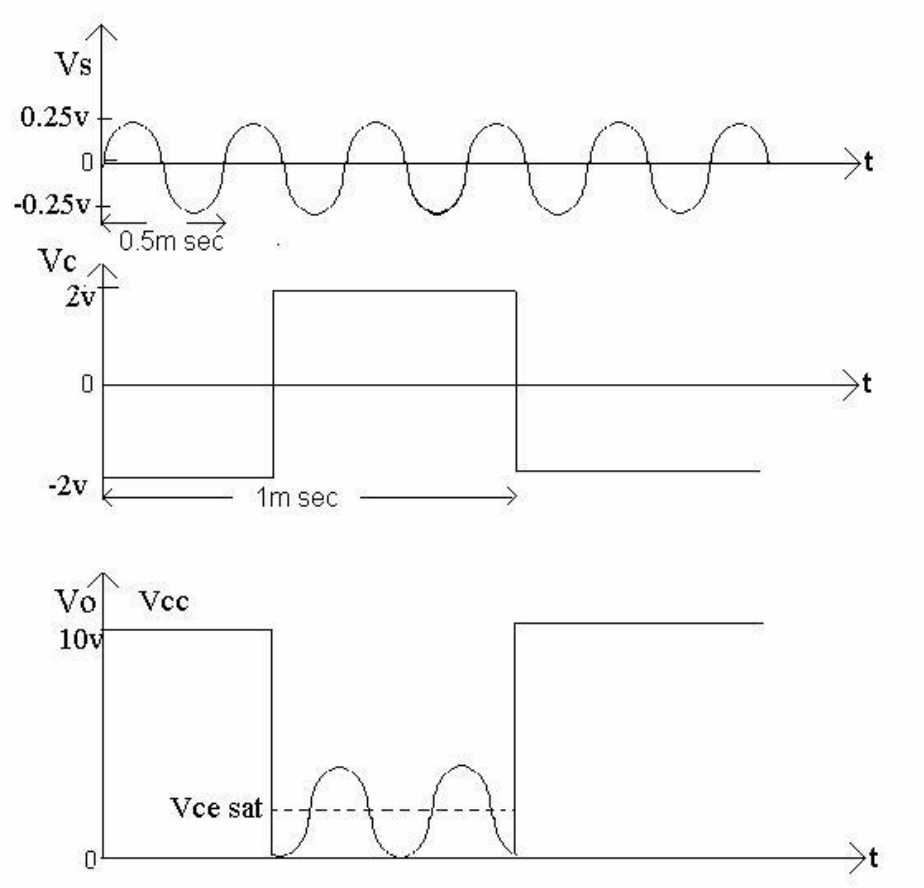
PROCEDURE:

1. Connect the circuit as per the diagram.
2. Generate a control voltage Vc of 4V peak to peak voltage 1KHz and apply it to the circuit.
3. Apply the input signal with a small peak to peak voltage.

4 Observe the output wave forms and Vc simultaneously and note down the parameters of waveforms.

5.Plot the graph between $V_{s,}V_c$ and output waveform with respect to time

MODEL WAVE FORMS:



PRECAUTIONS:

1. Connections must be done carefully.
2. Observe the output waveforms with out parallax error

RESULT:

The performance of the sampling gate is observed.

INFERENCE:

Sampling gates, also called linear gates transmission gates or selection circuits are transmission circuits in which the output is an exact reproduction of the input during a selected time interval and is zero otherwise. The time interval for transmission is selected by an extremely impressed signal which is called the gating signal and usually rectangular in wave shape.

QUESTION & ANSWERS:

1. What are the other names of sampling gates?

Ans. Linear gate, transmission gate.

2. What do you meant by pedestal?

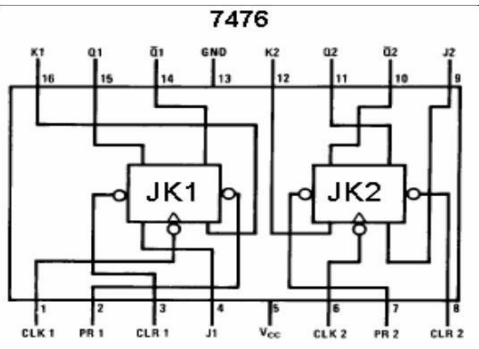
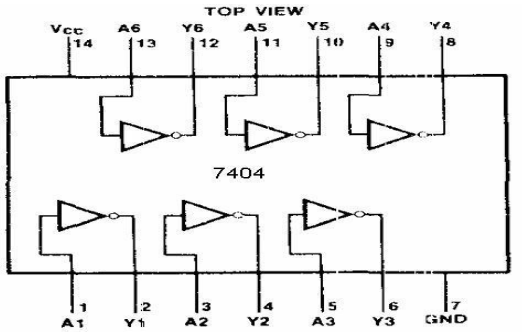
Ans. Pedastal is the base voltage in the output on which the input siganal is superimposed.

3. What are the applications of sampling gates?

Ans. Multiplexers, Sample &Hold circuit, digital to analog converter.

APPENDIX

<table>
<tr><th>Name of The Component</th><th colspan="2">Specifications/Pin Diagrams</th></tr>
<tr><td>Transistor
(BC 107)</td><td colspan="2">* operating point temp-65^o to 200^o
* I_C(max)= 0.2 Amp
* h_{fe} (min) = 40
* h_{fe} (max) = 450</td></tr>
<tr><td rowspan="5">Uni Junction Transistor
(2N2646)</td><td>Ic</td><td>2.0A(Pulsed)</td></tr>
<tr><td>Vce</td><td>30V</td></tr>
<tr><td>PDISS</td><td>300mW@$T_{C=}$25ºC</td></tr>
<tr><td>TSTG</td><td>-65ºC to +150ºC</td></tr>
<tr><td>T_J</td><td>-65ºC to +125ºC</td></tr>
<tr><td colspan="3">Diodes
<table>
<tr><td>Type No</td><td>1N4001</td><td>1N4007</td></tr>
<tr><td>Max. Peak Inverse Volts</td><td>50</td><td>1000</td></tr>
<tr><td>Max RMS Supply Volts</td><td>35</td><td>700</td></tr>
<tr><td>Maximum Forward Voltage
@ 1Ampere, DC @ 75^0 C</td><td colspan="2">1.1 Volts,Peak</td></tr>
<tr><td>Maximum Reverse DC Current
@PIV @ 25^0 C</td><td colspan="2">10µA</td></tr>
<tr><td>Maximum Dynamic Reverse Current
@PIV @75^0 C</td><td colspan="2">30µA,Average</td></tr>
</table></td></tr>
</table>

IC 7476	
IC 7404	

REFERENCES:

1.Pulase and digital circuits- J.Milliman and H.Taub,McGraw-Hill 2.Solid State Pulse circuits-David A.Bell,PHI

3.Pulse and Digital Circuits-A.Anand Kumar,PHI 4.www.analog.com 5.www.datasheetarchive.com

6.www.ti.com

ELECTRICAL TECHNOLOGY

LABORATORY MANUAL

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG.

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous Institution-UGC, Govt. of India

(Sponsored by CMR Educational Society)

(Affiliated to JNTU, Hyderabad)

Secunderabad- 500010.

ELECTRONICS & COMMUNICATION ENGINEERING

VISION

To evolve into a centre of excellence in Engineering Technology through creative and innovative practices in teaching-learning, promoting academic achievement & research excellence to produce internationally accepted competitive and world class professionals.

MISSION

To provide high quality academic programmes, training activities, research facilities and opportunities supported by continuous industry institute interaction aimed at employability, entrepreneurship, leadership and research aptitude among students.

QUALITY POLICY

- Impart up-to-date knowledge to the students in Electronics & Communication area to make them quality engineers.
- Make the students experience the applications on quality equipment and tools.
- Provide systems, resources and training opportunities to achieve continuous improvement.
- Maintain global standards in education, training and services.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO1: PROFESSIONALISM & CITIZENSHIP

To create and sustain a community of learning in which students acquire knowledge and learn to apply it professionally with due consideration for ethical, ecological and economic issues.

PEO2: TECHNICAL ACCOMPLISHMENTS

To provide knowledge based services to satisfy the needs of society and the industry by providing hands on experience in various technologies in core field.

PEO3: INVENTION, INNOVATION AND CREATIVITY

To make the students to design, experiment, analyze, interpret in the core field with the help of other multi disciplinary concepts wherever applicable.

PEO4: PROFESSIONAL DEVELOPMENT

To educate the students to disseminate research findings with good soft skills and become a successful entrepreneur.

PEO5: HUMAN RESOURCE DEVELOPMENT

To graduate the students in building national capabilities in technology, education and research**.**

PROGRAMME SPECIFIC OBJECTIVES (PSOs)

PSO1

To develop a student community who acquire knowledge by ethical learning and fulfill the societal and industry needs in various technologies of core field.

PSO2

To nurture the students in designing, analyzing and interpreting required in research and development with exposure in multi disciplinary technologies in order to mould them as successful industry ready engineers/entrepreneurs

PSO3

To empower students with all round capabilities who will be useful in making nation strong in technology, education and research domains.

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design / development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multi disciplinary environments.
12. **Life- long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

LIST OF EXPERIMENTS

PART- A

PART- B

1. VERIFICATION OF KIRCHOFF'S LAWS

AIM: To verify the Kirchhoff's voltage law and Kirchhoff's current law for the given circuit.

APPARATUS REQUIRED:

S.No	Name of the equipment	Range	Type	Quantity
1	RPS	0-30V	-	1N0
2	Voltmeter	0-20 V	Digital	4 NO
3	Ammeter	0-20mA	Digital	4 NO
4	Bread board	-	-	1 NO
5	Connecting wires	-	-	Required number.
6	Resistors	470 Ω		2 NO
		1kΩ		1 NO
		680Ω		1 NO

CIRCUIT DIAGRAMS:

GIVEN CIRCUIT:

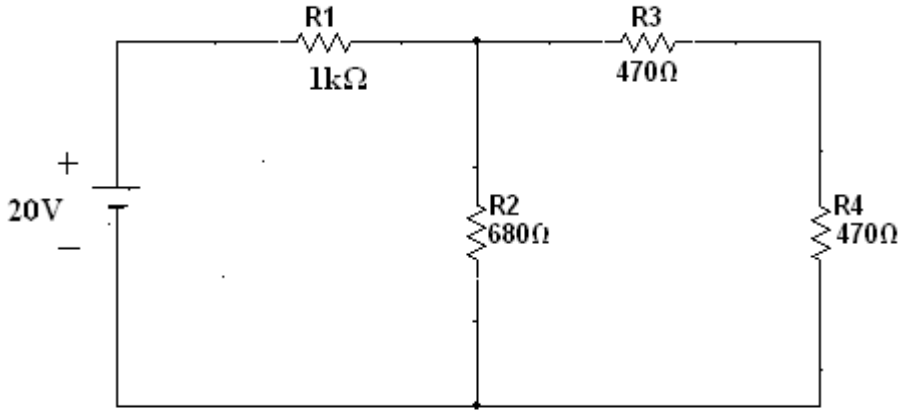


Fig (1)

1. KVL:

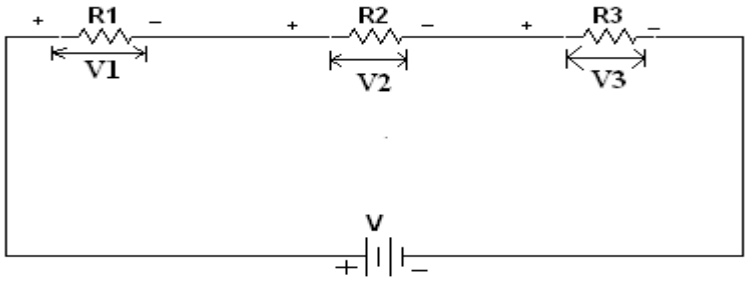
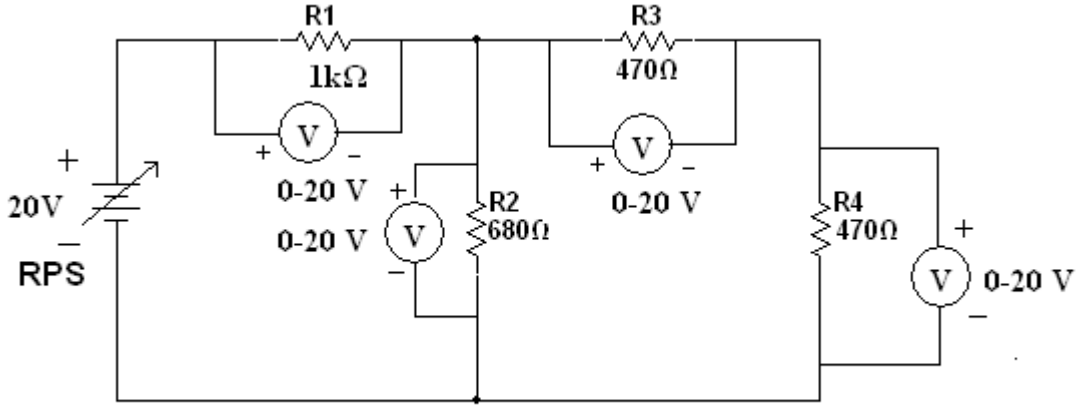


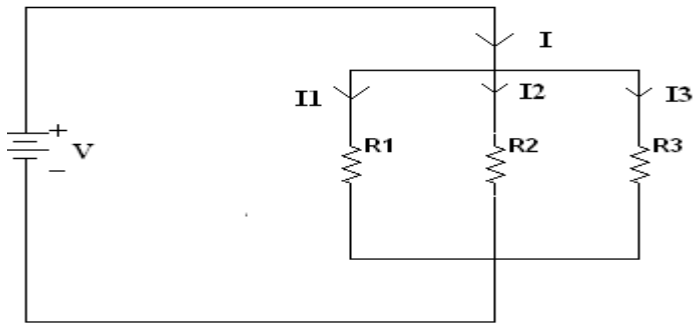
Fig (1a)

PRACTICAL CIRCUIT:



Fig(2 a)

2. KCL:



Fig(1b)

PRACTICAL CIRCUIT:

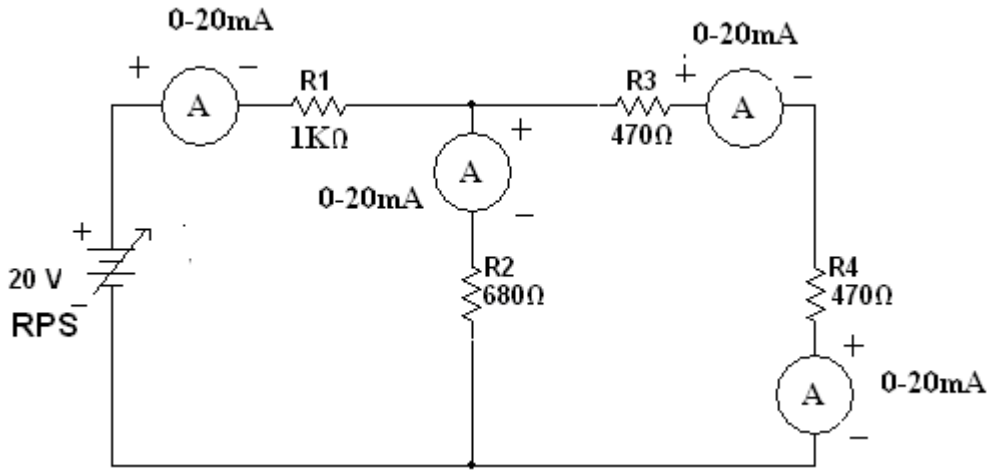


Fig (2b)

THEORY:

a) Kirchhoff's Voltage law states that the algebraic sum of the voltage around any closed path in a given circuit is always zero. In any circuit, voltage drops across the resistors always have polarities opposite to the source polarity. When the current passes through the resistor, there is a loss in energy and therefore a voltage drop. In any element, the current flows from a higher potential to lower potential. Consider the fig (1a) shown above in which there are 3 resistors are in series. According to kickoff's voltage law….

$$\mathbf{V = V_1 + V_2 + V_3}$$

b) Kirchhoff's current law states that the sum of the currents entering a node equal to the sum of the currents leaving the same node. Consider the fig (1b) shown above in which there are 3 parallel paths. According to Kirchhoff's current law...

$$\mathbf{I = I_1 + I_2 + I_3}$$

PROCEDURE:

a) Kirchhoff's Voltage law:
   1. Connect the circuit as shown in fig (2a).
   2. Measure the voltages across the resistors.
   3. Observe that the algebraic sum of voltages in a closed loop is zero.

b) Kirchhoff's current law:
   1. Connect the circuit as shown in fig (2b).
   2. Measure the currents through the resistors.
   3. Observe that the algebraic sum of the currents at a node is zero.

OBSERVATION TABLE:

KVL:

S.NO	VOLTAGE ACROSS RESISTOR	THEORETICAL	PRACTICAL

KCL:

S.NO	CURRENT THROUGH RESISTOR	THEORETICAL	PRACTICAL

PRECAUTIONS:

1. Avoid loose connections.
2. Keep all the knobs in minimum position while switch on and off of the supply.

RESULT:

QUESTIONS:

1. What is another name for KCL & KVL?
2. Define network and circuit?
3. What is the property of inductor and capacitor?

2. SERIES AND PARALLEL RESONANCE

AIM: To find the resonant frequency, quality factor and band width of a given series and parallel resonant circuits.

APPARATUS REQUIRED:

S. No.	Apparatus	Range	Type	Quantity
1	Bread board	-	-	1
2	Resistor		-	1
3	Inductor	1k Ω	-	1
4	Capacitor	50 mH	-	1
5	CRO	0.1uF	-	1
6	Function	20MHz.Dual CH	-	1
7	generator	100-10MHz	-	1
8	Ammeter	0-20mA	Digital	1
9	Connecting wires			Required number

CIRCUIT DIAGRAM:

SERIES RESONANCE:

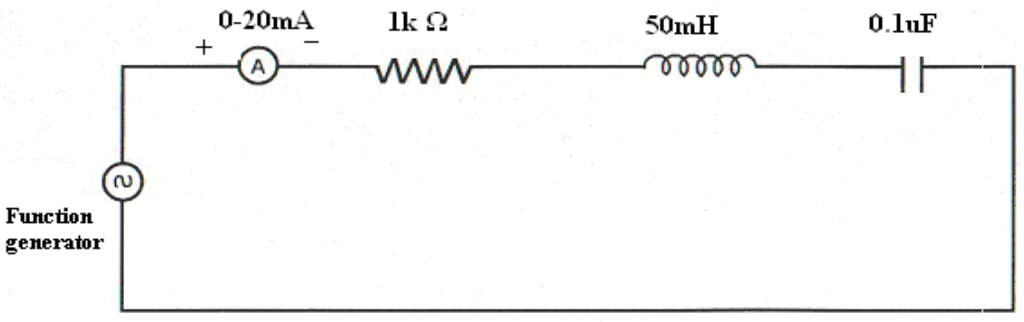


Fig.1

PARALLEL RESONANACE*:*

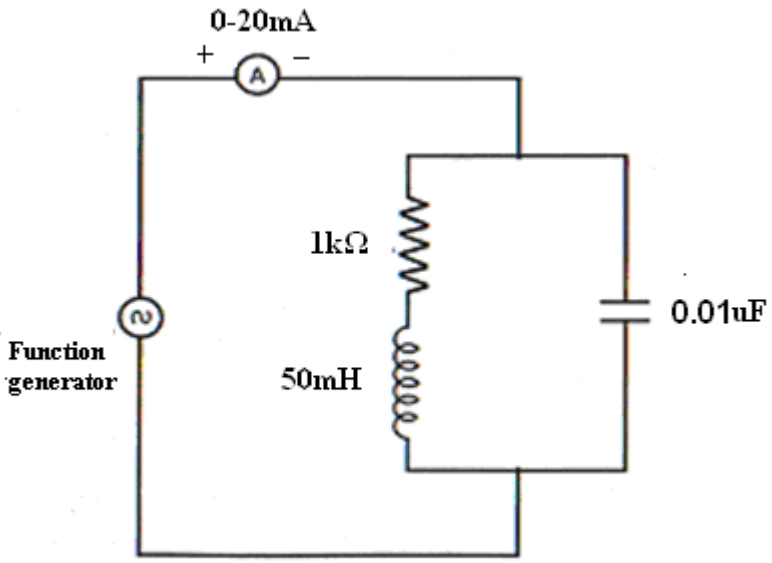


Fig.2

THEORY:

Resonance is a particular type of phenomenon inherently found normally in every kind of system, electrical, mechanical, optical, Acoustical and even atomic. There are several definitions of resonance. But, the most frequently used definition of resonance in electrical system is studied state operation of a circuit or system at that frequency for which the resultant response is in time phase with the forcing function.

SERIES ROSONACE:

A circuit is said to be under resonance, when the applied voltage 'V' and current are in phase. Thus a series RLC circuit, under resonance behaves like a pure resistance network and the reactance of the circuit should be zero. Since V & I are in phase, the power factor is unity at resonance.

The frequency at which the resonance will occur is known as resonant frequency**.** Resonant frequency,

$$fr = \frac{1}{2 \prod \sqrt{L C}}$$

Thus at resonance the impedance Z is minimum. Since I = V/Z. The current is maximum So that current amplification takes place. Quality factor is the ratio of reactance power inductor (or) capacitor to its resistance.

PARALLEL RESONANCE:

The parallel circuit consisting branches with single pure elements R, L & C is an ideal circuit. How ever the performance of such a circuit is of interest in the general subject of resonance. At resonance impedance is maximum and the voltage is maximum.

This ideal parallel circuit is of interest in the general subject of resonance.Lower cut-off frequency is above the resonant frequency at which the current is reduced to $\frac{1}{\sqrt{2}}$ times of its minimum value. Upper cut-off frequency is above.

Quality factor is the ratio of resistance to reactance of inductor (or) capacitor. Selectivity is the reciprocal of the quality factors.

THEORITICAL CALCULATIONS:

For Series Resonance circuit:

1. Resonant frequency $f_r = \frac{1}{2\pi\sqrt{LC}}$
2. Lower cut-off frequency $f_l = \frac{1}{2\pi}\left[\frac{-R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}\right]$
3. Upper cut-off frequency $f_2 = \frac{1}{2\pi}\left[\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 + \frac{1}{LC}}\right]$
4. Band width = f_2-f_1:
5. Quality factor $Q = \frac{w_0 L}{R} = \frac{2\pi fr.L}{R}$
6. Current at Resonance $I_o = V_{Ro}/R$

For Parallel Resonance circuit:

1. Resonant frequency $f_r = \frac{1}{2\pi}\sqrt{\left(\frac{1}{LC}\right) - \left(\frac{R}{L}\right)^2}$
2. Lower cut-off frequency $f_l = \frac{1}{2\pi}\left[-\frac{R}{2L} + \frac{1}{2}\sqrt{\left(\frac{R}{L}\right)^2 + \left(\frac{4}{LC}\right)}\right]$
3. Upper cut-off frequency $f_2 = \frac{1}{2\pi}\left[\frac{R}{2L} + \frac{1}{2}\sqrt{\left(\frac{R}{L}\right)^2 + \left(\frac{4}{LC}\right)}\right]$
4. Band width = f_2-f_1:
5. Quality factor_Q = $\frac{R}{WoL}$
6. Current at resonance $I_o = V_{Ro}/R$

PROCEDURE:

1. Connect the circuit as shown in fig.1 for series resonant circuit & fig.2 for parallel resonant circuit.
2. Set the voltage of the signal from function generator to 5V.
3. Vary the frequency of the signal over a wide range in steps and note down the corresponding ammeter readings.
4. Observe that the current first increases & then decreases in case of series resonant circuit & the value of frequency corresponding to maximum current is equal to resonant frequency.

5. Observe that the current first decreases & then increases in case of parallel resonant circuit & the value of frequency corresponding to minimum current is equal to resonant frequency.
6. Draw a graph between frequency and current & calculate the values of bandwidth & quality factor.

OBSERVATION TABLE:
Series Resonance:

S. No.	**Frequency** (Hz)	**Current** (mA)

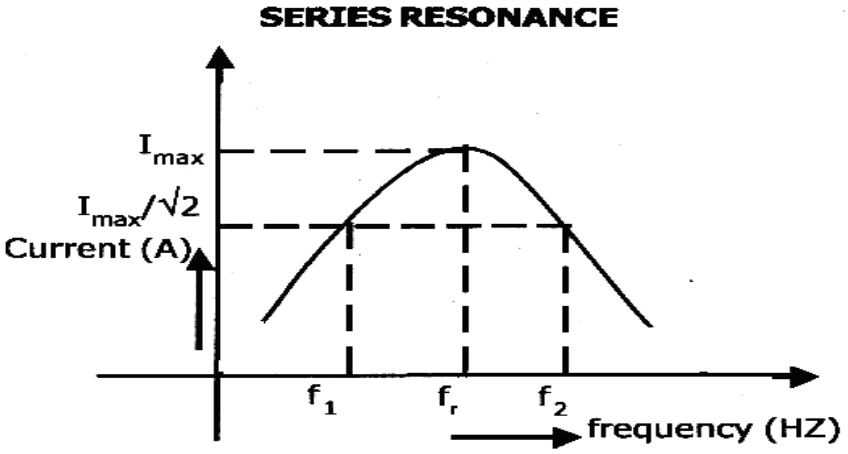
OBSERVATION TABLE:
Parallel Resonance:

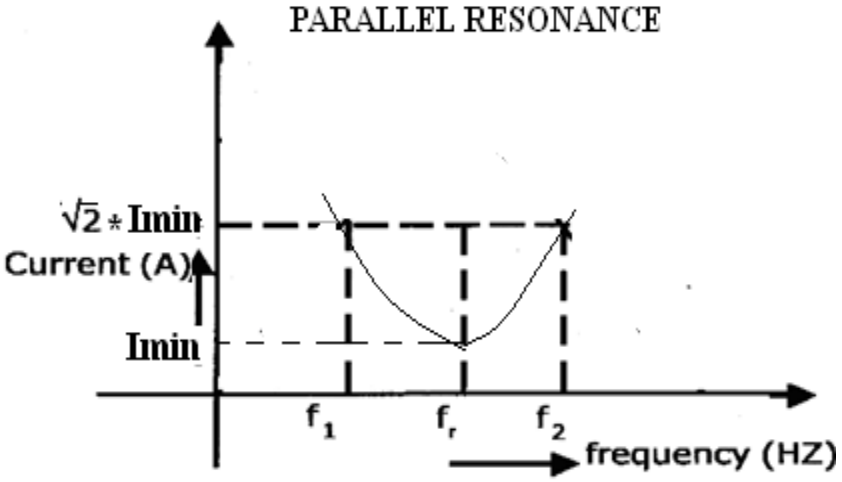
S. No.	**Frequency** (Hz)	**Current** (mA)

TABULAR COLUMN:

S.NO	**PARAMETER**	**Series resonant circuit**		**Parallel resonant circuit**	
		Theoretical	**Practical**	**Theoretical**	**Practical**
1	Resonant Frequency(fr)				
2	Band width				
3	Quality factor				

MODEL GRAPHS:





f1= lower cutoff frequency
f2 = upper cutoff frequency
fr=Resonant Frequency

OBSERVATIONS:

1. Since the current at resonance is maximum, the series resonant circuit is called as acceptor circuit.
2. As the resistance of the circuit decreases, the Q-factor increases and selectivity of the circuit will be better.
3. Since the current at resonance is minimum, the parallel resonant circuit is called as rejecter circuit.
4. The variation of the resistance does not affect the resonant frequency.

RESULT:

QUESTIONS:

1) What is resonance of circuit?
2) What is series and parallel resonance?

3. DETERMINATION OF Z AND Y PARAMETERS OF A TWO- PORT NETWORK

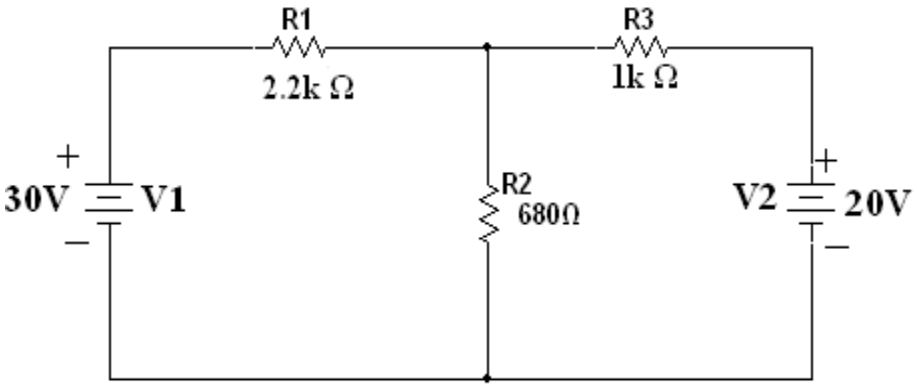
AIM: To determine the Impedance (Z) and admittance (Y) parameters of a two port network.

APPARATUS REQUIRED:

S.No	Name Of The Equipment	Range	Type	Quantity
1	Voltmeter	(0-20)V	Digital	1 NO
2	Ammeter	(0-20)mA	Digital	1 NO
3	RPS	0-30V	Digital	1 NO
4	Resistors	2.2k Ω	-	1 NO
		1k Ω	-	1 NO
		680 Ω	-	1 NO

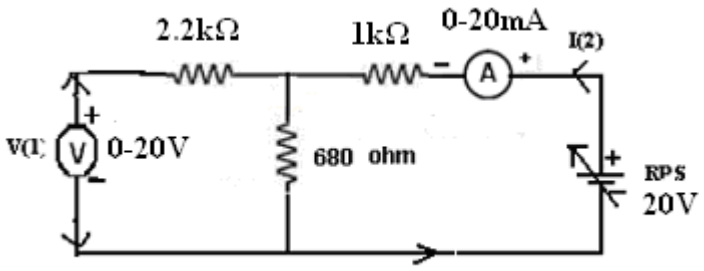
CIRCUIT DIAGRAMS:

1. GIVEN CIRCUIT:

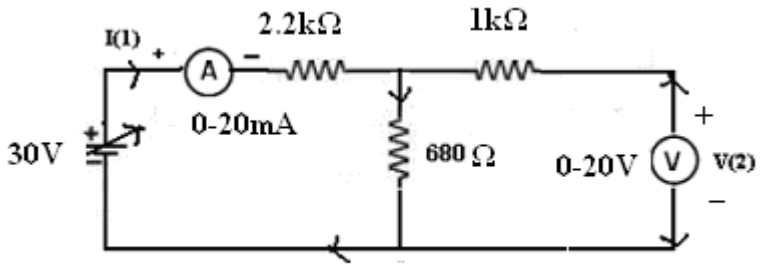


PRACTICAL CIRCUITS:

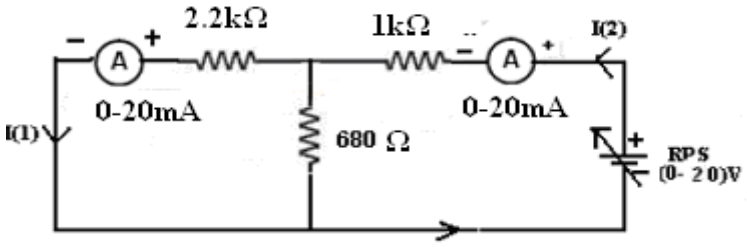
2. When I_1 = 0:



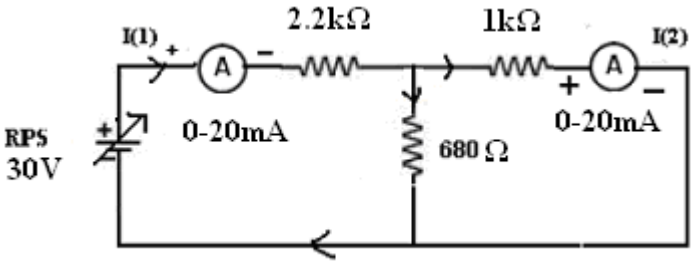
3. When I_2 = 0:



4. When V_1 = 0:



5. When V_2 = 0:



THEORY:

A pair of terminals between which a signal may enter or leave the network is known as port. If a network has one such type pair of terminals it is known as One-Port Network and that have two such type of ports is known as Two-Port Network.

If we relate the voltage of one port to the current of the same port, we get driving point admittance. On the other hand, if we relate the voltage of one port to the current at another port, we get transfer admittance. Admittance is a general term used to represent either the impedance or the admittance of a network. We will consider a general two-port network composed of linear, bilateral elements and no independent sources. The voltage and current at port -1 are V_1 and I_1 and at port -2 are V_2 and I_2. The position of V_1 and V_2 and the directions of I_1 and I_2 are customarily selected. Out of four variables only two are independent. The other two are expressed in terms of the independent variable of network parameters.The relation between the voltages and currents in terms of Z and Y parameters are as follows.

$V_1=Z_{11}(I_1)+Z_{12}(I_2)$

$V_2=Z_{21}(I_1)+Z_{22}(I_2)$

$I_1=Y_{11}(V_1)+Y_{12}(V_2)$

$I_2=Y_{21}(V_1)+Y_{22}(V_2)$

Z-PARAMETERS:

$Z11 = \frac{V1}{I1} / I_2 = 0$

$Z12 = \frac{V1}{I2} / I_1 = 0$

$Z21 = \frac{V2}{I1} / I_2 = 0$

$Z22 = \frac{V2}{I2} / I_1 = 0$

Y-PARAMETERS:

$$Y11 = \frac{I1}{V1} / V2 = 0$$

$$Y12 = \frac{I2}{V1} / V1 = 0$$

$$Y21 = \frac{I2}{V1} / V2 = 0$$

$$Y22 = \frac{I2}{V2} / V1 = 0$$

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Open circuit the port – 1 i.e., $I_1=0$, find the values ofV_1, I2 and V_2.
3. Short circuit the port-1 i.e. $V_1=0$, find the values of V_2, $I_1$and I_2.
4. Open circuit the port – 2 i.e., $I_2=0$, find the values of V_1, I1 and V_2.
5. Short circuit the port-2 i.e. $V_2=0$, find the values of V_1, $I_1$and I_2.
5. Find the Z and Y parameters of the given two port network.

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THEORITICAL VALUES:

$V_1 = 0$	$V_{2=}$	$I_{1=}$	$I_{2=}$
$V_2 = 0$	$V_{1=}$	$I_{1=}$	$I_{2=}$
$I_1 = 0$	$V_{1=}$	$V_{2=}$	$I_{2=}$
$I_2 = 0$	$V_{1=}$	$V_{2=}$	$I_{1=}$

PRACTICAL VALUES:

$V_1 = 0$	$V_{2=}$	$I_{1=}$	$I_{2=}$
$V_2 = 0$	$V_{1=}$	$I_{1=}$	$I_{2=}$
$I_1 = 0$	$V_{1=}$	$V_{2=}$	$I_{2=}$
$I_2 = 0$	$V_{1=}$	$V_{2=}$	$I_{1=}$

Z-PARAMETERS:

Z-parameters	Theoretical	Practical
$Z11 = \frac{V1}{I1}$ / I_2 =0		
$Z12 = \frac{V1}{I2}$ / I_1 =0		
$Z21 = \frac{V2}{I1}$ / I_2 =0		
$Z22 = \frac{V2}{I2}$ / I_1 =0		

Y-PARAMETERS:

Y-Parameters	Theoretical	Practical
$Y11 = \frac{I1}{V1} / V2 = 0$		
$Y12 = \frac{I2}{V1} / V1 = 0$		
$Y21 = \frac{I2}{V1} / V2 = 0$		
$Y22 = \frac{I2}{V2} / V1 = 0$		

PRECAUTIONS:

1. Initially keep the RPS output voltage knob in zero volt position.
2. Set the ammeter pointer to zero position.
3. Take the readings without parallax error.
4. Avoid loose connections.
5. Do not short-circuit the RPS output terminals.

RESULT:

QUESTIONS:

1. Define Port?
2. Define z,y parameters?
3. What is the condition for symmetry in case Z & Y parameters?
4. Define characteristic impedance?
5. What is the condition for reciprocity in case Z & Y parameters?

4. DETERMINATION OF ABCD (T) AND HYBRID (h) PARAMETERS OF A TWO-PORT NETWORK

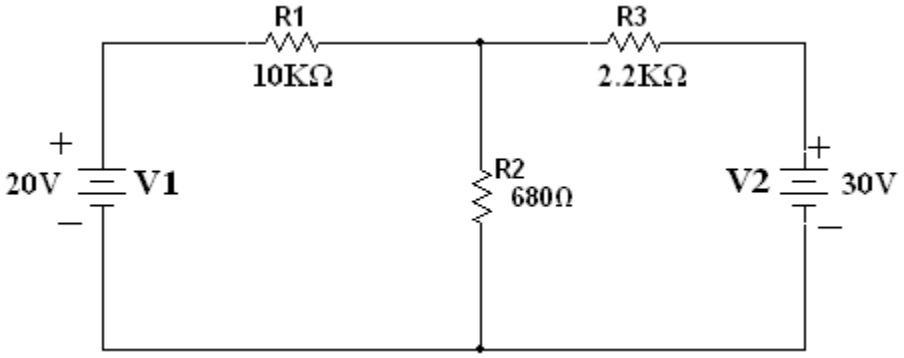
AIM: To determine the ABCD (T) and Hybrid (h) parameters of a two port network.

APPARATUS REQUIRED:

S.No	Name Of The Equipment	Range	Type	Quantity
1	Voltmeter	(0-20)V	Digital	1 NO
2	Ammeter	(0-20)mA	Digital	1 NO
3	RPS	0-30V	Digital	1 NO
4	Resistors	10K Ω		1 NO
		2.2Ω		1 NO
		680 Ω		1 NO
5	Breadboard	-	-	1 NO
6	Connecting wires			Required number

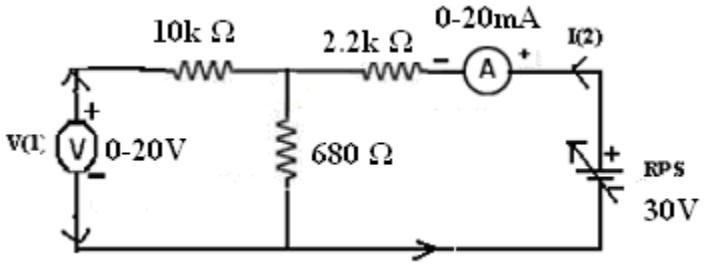
CIRCUIT DIAGRAMS:

GIVEN CIRCUIT:

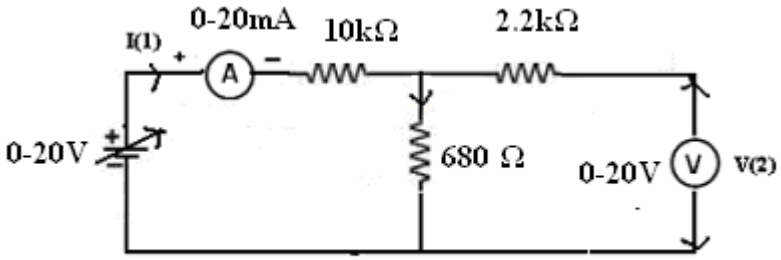


PRACTICAL CIRCUITS:

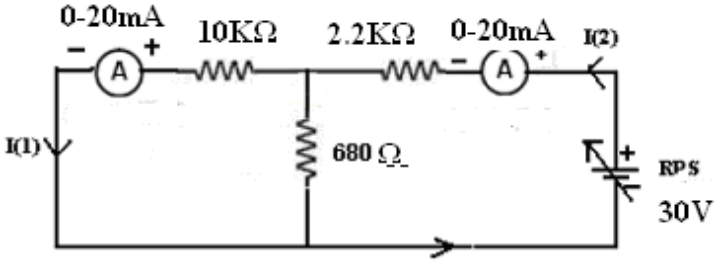
1. When I_1 = 0:



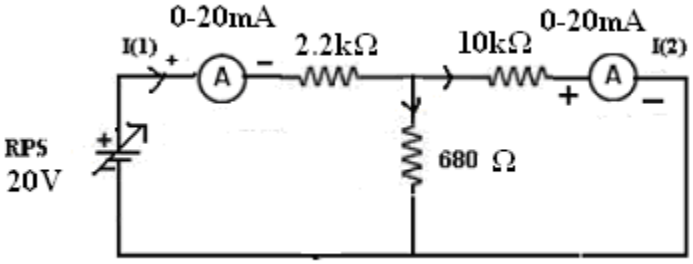
2. When I_2 = 0:



3. When V_1 = 0:



4. When V_2 = 0:



THEORY:
The relation between the voltages and currents of a two port network in terms of ABCD and h–parameters is given as follows.

ABCD PARAMETERS:

$V_1 = AV_2 - BI_2$
$I_1 = CV_2 - DI_2$

h-PARAMETERS

$V_1 = h_{11}I_1 + h_{12}V_2$
$I_2 = h_{11}I_1 + h_{22}V_2$

ABCD PARAMETERS:
$A = \frac{V1}{V2}$ / I2 =0
$B = \frac{-V1}{I2}$ / $V2$ =0
$C = \frac{I1}{V2}$ / I2 =0
$D = \frac{-I1}{I2}$ / V2 =0

h-PARAMETERS:

$h11 = \frac{V1}{I1}$ / V2 =0
$h12 = \frac{V1}{V2}$ / I1 =0
$h21 = \frac{I2}{I1}$ / V2 =0
$h22 = \frac{I2}{V2}$ / I1 =0

PROCEDURE:
1. Connections are made as per the circuit diagram.
2. Open circuit the port – 1 i.e., I_1=0 find the values ofV_1, I2 and V_2.
3. Short circuit the port-1 V_1 =0 find the values of V_2, $I_1$and I_2.
4. Open circuit the port – 2 i.e., I_2=0 find the values of V_1, I1 and V_2.
5. Short circuit the port-2 i.e. V_2 =0 find the values of V_1, $I_1$and I_2
5. Find the ABCD and h-parameters of the given two port network from the above data.

THEORITICAL VALUES:

V_1 = 0	$V_{2=}$	$I_{1=}$	$I_{2=}$
V_2 = 0	$V_{1=}$	$I_{1=}$	$I_{2=}$
I_1 = 0	$V_{1=}$	$V_{2=}$	$I_{2=}$
I_2 = 0	$V_{1=}$	$V_{2=}$	$I_{1=}$

PRACTICAL VALUES:

$V_1 = 0$	$V_{2=}$	$I_{1=}$	$I_{2=}$
$V_2 = 0$	$V_{1=}$	$I_{1=}$	$I_{2=}$
$I_1 = 0$	$V_{1=}$	$V_{2=}$	$I_{2=}$
$I_2 = 0$	$V_{1=}$	$V_{2=}$	$I_{1=}$

ABCD-PARAMETERS:

T-parameters	Theoretical	Practical
$A = \frac{V1}{V2}$ / I_2 =0		
$B = \frac{-V1}{I2}$ / $V2$ =0		
$C = \frac{I1}{V2}$ / I_2 =0		
$D = \frac{-I1}{I2}$ / V_2 =0		

h- PARAMETERS:

h-Parameters	Theoretical	Practical
$h11 = \frac{V1}{I1}$ / V_2 =0		
$h12 = \frac{V1}{V2}$ / I_1 =0		
$h21 = \frac{I2}{I1}$ / V_2 =0		
$h22 = \frac{I2}{V2}$ / I_1 =0		

PRECAUTIONS:

1. Initially keep the RPS output voltage knob in zero volt position.
2. Set the ammeter pointer to zero position.
3. Take the readings without parallax error.

RESULT:

QUESTIONS;

1. Define Port?
2. Define image impedance?
3. What is the condition for symmetry in case h-parameters & ABCD (T) parameters?
4. Define characteristic impedance?
5. What is the condition for reciprocity in case Hybrid (h) & ABCD (T) parameters?

5. SUPERPOSITION AND RECIPROCITY THEOREM

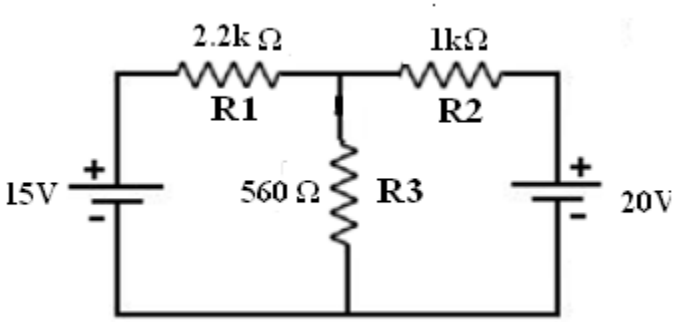
A) VERIFICATION OF SUPERPOSITION THEOREM

AIM: To verify the superposition theorem for the given circuit.

APPARATUS REQUIRED:

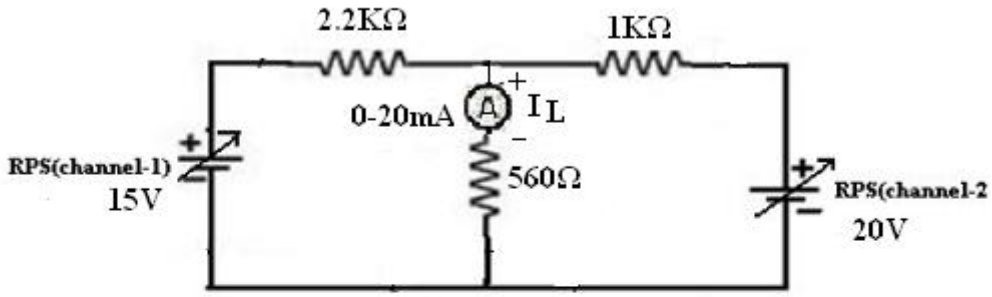
S.No	Name Of The Equipment	Range	Type	Quantity
1	Bread board	-	-	1 NO
2	Ammeter	(0-20)mA	Digital	1 NO
3	RPS	0-30V	Digital	1 NO
4	Resistors	2.2k Ω		1 NO
		1k Ω		1 NO
		560 Ω		1 NO

CIRCUIT DIAGRAM:



PRACTICAL CIRCUITS:

When V_1 & V_2 source acting(To find I):-



Fig(1)

When V_1 source acting(To find I_1):-

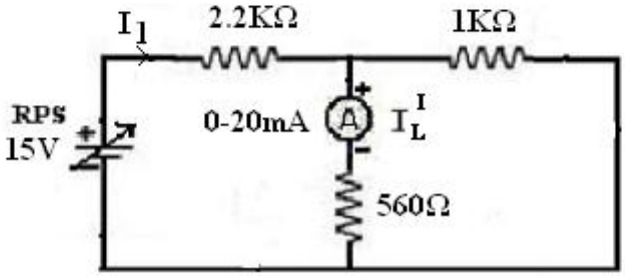


Fig (2)

When V2 source acting (To find I_2):

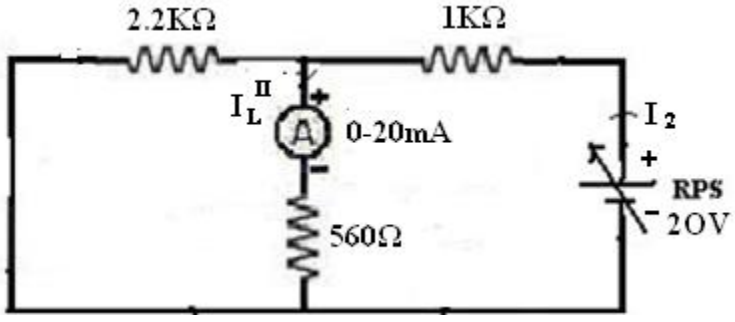


Fig (3)

THEORY:

SUPERPOSITION THEOREM:

Superposition theorem states that in a lumped ,linear, bilateral network consisting more number of sources each branch current(voltage) is the algebraic sum all currents (branch voltages), each of which is determined by considering one source at a time and removing all other sources. In removing the sources, voltage and current sources are replaced by internal resistances.

PROCEDURE:

1. Connect the circuit as per the fig (1).
2. Adjust the output voltage of sources X and Y to appropriate values (Say 15V and20V respectively).
3. Note down the current (I_L) through the 560 0hm resistor by using the ammeter.
4. Connect the circuit as per fig (2) and set the source Y (20V) to 0V.
5. Note down the current ($I_L^{1)}$ through 560ohm resistor by using ammeter.
6. Connect the circuit as per fig93) and set the source X (15V) to 0V and source Y to 20V.
7. Note down the current (I_L^{II}) through the 560 ohm resistor branch by using ammeter.
8. Reduce the output voltage of the sources X and Y to 0V and switch off the supply.
9. Disconnect the circuit**.**

THEORITICAL CALCULATIONS

From Fig(2)

$$I_1=V_1/(R_1+(R_2//R_3))$$

$$I_L^{1}=I_1^{*}R_2/(R_2+R_3)$$

From Fig(3)

$$I_2=V_2/(R_2+(R_1//R_3)$$

$$I_L^{II}=I_2^{*}R_1/(R_1+R_3)$$

$$I_L = I_L^{1} + I_L^{II}$$

TABULAR COLUMNS:

From Fig(1)

S. No	Applied voltage (V_1) Volt	Applied voltage (V_2) Volt	Current I_L (mA)

From Fig(2)

S. No	Applied voltage (V_1) Volt	Current I_L^I (mA)

From Fig(3)

S. No	Applied voltage (V_2) Volt	Current I_L^{II} (mA)

TABULER COLUMNS:

S.No	Load current	Theoretical Values	Practical Values
1	When Both sources are acting, I_L		
2	When only source X is acting, I_L^1		
3	When only source Y is acting, I_L^{II}		

PRECAUTIONS:

1. Initially keep the RPS output voltage knob in zero volt position.
2. Set the ammeter pointer at zero position.
3. Take the readings without parallax error.

4. Avoid loose connections.
5. Avoid short circuit of RPS output terminals.

RESULT:

QUESTIONS:

1) What do you man by Unilateral and Bilateral network? Give the limitations of superposition theorem?
2) What are the equivalent internal impedances for an ideal voltage source and for a Current source?
3) Transform a physical voltage source into its equivalent current source.
4) If all the 3 star connected impedance are identical and equal to ZA, then what is the Delta connected resistors?

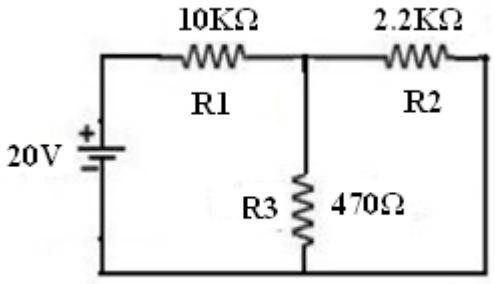
(B)RECIPROCITY THEOREM

AIM: To verify reciprocity theorem for the given circuit.

APPARATUS REQUIRED:

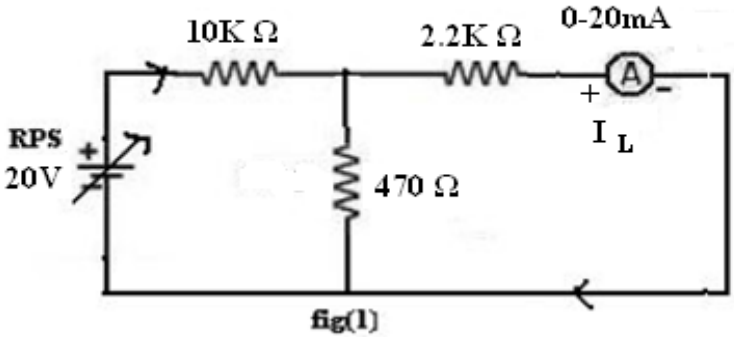
S.No	Name Of The Equipment	Range	Type	Quantity
1	Bread board	-	-	1 NO
2	Ammeter	(0-20)mA	Digital	1 NO
3	RPS	0-30V	Digital	1 NO
4	Resistors	2.2k Ω		1 NO
		10k Ω		1 NO
		470 Ω		1 NO

CIRCUIT DIAGRAM:



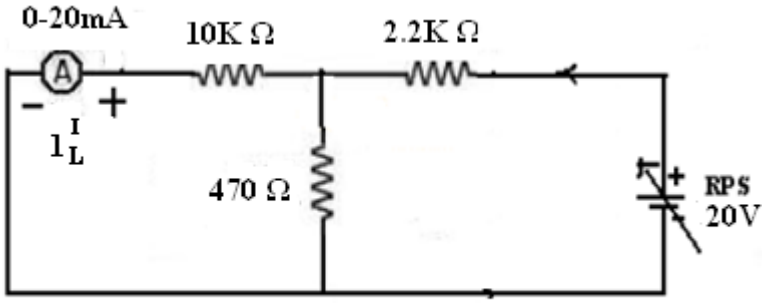
PRACTICAL CIRCUITS:

CIRCUIT – 1:



fig(1)

CIRCUIT-2:



fig(2)

THEORY:

STATEMENT:

In any linear, bilateral, single source network, the ratio of response to the excitation is same even though the positions of excitation and response are interchanged.

This theorem permits in to transfer source from one position in the circuit to another and may be stated as under.
In any linear bilateral network, if an e.m.f acting in a branch causes a current 'I' in branch 'Y' then the same e.m.f E located in branch 'Y' will cause a current I in branch. However, currents in other branches will not change.

PROCEDURE:

1. Connect the circuit as per the fig (1).
2. Adjust the output voltage of the regulated power supply to an appropriate value (Say 20V).
3. Note down the current through 2.2K Ω by usingammeter.
4. Reduce the output voltage of the RPS to 0V and switch-off the supply.

5. Disconnect the circuit and connect the circuit as per the fig (2).
6. Adjust the output voltage of the regulated power supply to an appropriate value (Say 20V).
7. Note down the current through 10K Ω resistor from ammeter.
8. Reduce the output voltage of the RPS to 0V and switch-off the supply.
9. Disconnect the circuit.

THEORITICAL CALCULATIONS :

From Fig(1)

$$I_1=V/(R_1+(R_2//R_3))$$

$$I_L= I_1{}^*R_3/(R_2+R_3)$$

From Fig(2)

$$I_2=V/(R_2+(R_1//R_3))$$

$$I_L{}^1= I_2{}^*R_3/(R_1+R_3)$$

TABULAR COLUMNS:

From fig 1

S. No	Applied voltage (V1) Volt	Current I_L (mA)

From fig 2

S. No	Applied voltage (V2) Volt	Current $I_L{}^I$ (mA)

OBSERVATION TABLE:

S.No	Parameter	Theoretical Value	Practical Value
1	I_L /v1		
2	I_L^1/v2		

PRECAUTIONS:

1. Initially keep the RPS output voltage knob in zero volt position.
2. Set the ammeter pointer at zero position.
3. Take the readings without parallax error.
4. Avoid loose connections.
5. Avoid short circuit of RPS output terminals.
6. If voltmeter gives negative reading then interchange the terminals connections of a voltmeter

RESULT:

QUESTIONS:

1) What is reciprocity theorem?
2) Why it is not applicable for unilateral circuit?

6. MAXIMUM POWER TRANSFER THEOREM

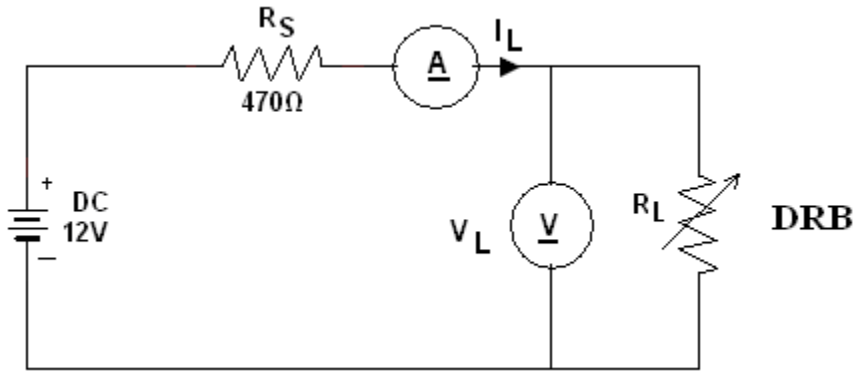
AIM:

To verify the maximum power transfer theorem for the given circuit.

APPARTUS REQUIRED:

SI. No	Equipment	Range	Qty
1	Bread board	-	1
2	DC Voltage source.	0-30V	1
3	Resistors	470 Ω	1
4	Decade resistance box	0-10k Ω	1
5	Ammeter	0-20mA	1
6	Voltmeter	0-20V	1
7	Connecting wires	1.0.Sq.mm	As required

CIRCUIT DIAGRAM:



THEORY:

STATEMENT:

It states that the maximum power is transferred from the source to load when the load resistance is equal to the internal resistance of the source.

(or)

The maximum transformer states that " A load will receive maximum power from a linear bilateral network when its load resistance is exactly equal to the Thevenin's resistance of network, measured looking back into the terminals of network.

Consider a voltage source of V of internal resistance R_i delivering power to a load Resistance R_L

$$\text{Circuit current} = \frac{V}{R_L + R_i}$$

$$\text{Power delivered } P = I^2 R_L$$

$$= \left|\frac{V}{R_L + R_i}\right|^2 R_L$$

$$\text{for maximum poewer } \frac{d(p)}{dt} = 0$$

RL+Ri cannot be zero,

$$Ri - RL = 0$$

$$\boxed{R_L == Ri}$$

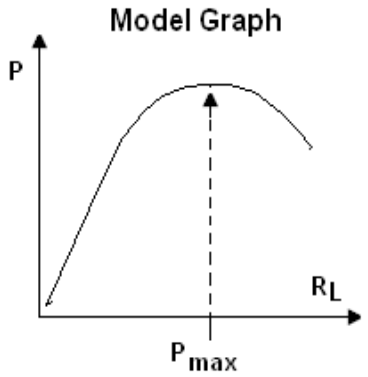
$$\mathbf{Pmax} = \frac{\mathbf{v2}}{\mathbf{4R_i}} \text{ watts}$$

PROCEDURE:

1. Connect the circuit as shown in the above figure.
2. Apply the voltage 12V from RPS.
3. Now vary the load resistance (R_L) in steps and note down the corresponding Ammeter Reading (I_L)in milli amps and Load Voltage (V_L) volts
6. Tabulate the readings and find the power for different load resistance values.
7. Draw the graph between Power and Load Resistance.
8. After plotting the graph, the Power will be Maximum, when the Load Resistance will be equal to source Resistance

TABULAR COLUMN:

S.No	I_L(mA)	V_L(Volts)	$R=V_L/I_L$ (Ω)	Power(P max)=I^2*R_L(mW)
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				



Theoretical Calculations:-

R = $(R_i + R_L)$=……..**Ω**

I = **V** / R =……..…….**mA**

Power = (I^2) $\mathbf{R_i}$ =…..…..**mW**

RESULT:

QUESTIONS:

1) What is maximum power transfer theorem?
2) What is the application this theorem?

7. VERIFICATION OF THEVENIN'S THEOREM AND NORTON'S THEOREM

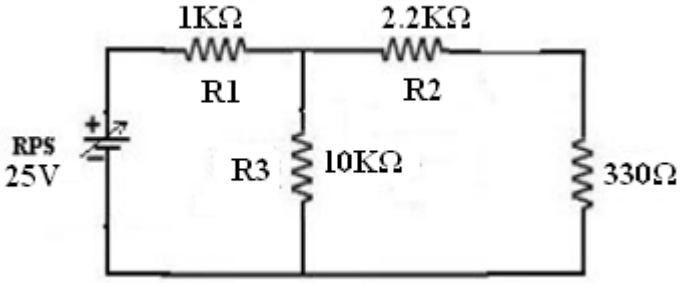
AIM: To verify Theremin's & Norton's theorems for the given circuit.

APPARATUS REQUIRED:

S.No	Name Of The Equipment	Range	Type	Quantity
1	Voltmeter	(0-20)V	Digital	1 NO
2	Ammeter	(0-20)mA	Digital	1 NO
3	RPS	0-30V	Digital	1 NO
4	Resistors	10K Ω,1K Ω		1 NO
		2.2Ω		1 NO
		330 Ω		1 NO
5	Breadboard	-	-	1 NO
6	Connecting wires			Required number

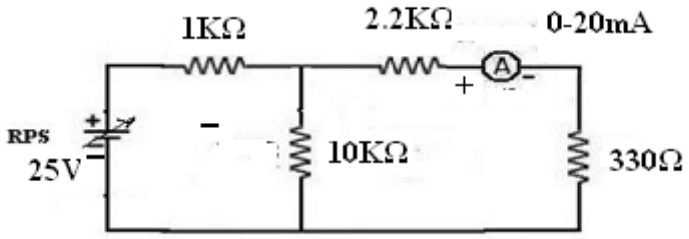
CIRCUIT DIAGRAM:

GIVEN CIRCUIT:



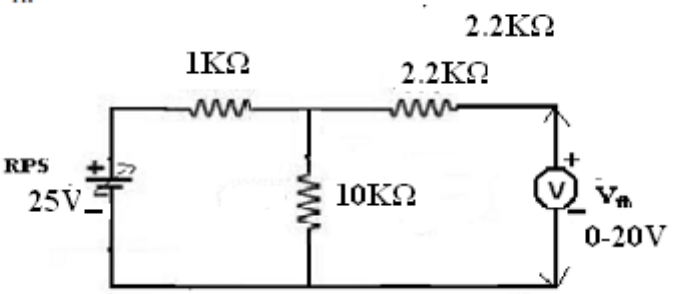
PRACTICAL CIRCUIT DIAGRAMS:

TO FIND I_L:



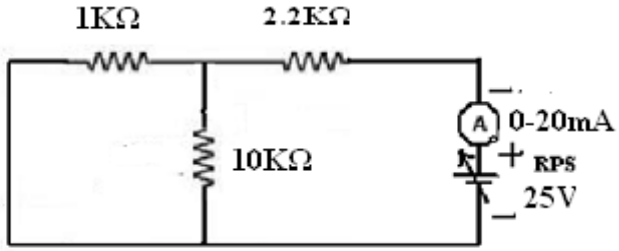
FIG(1)

TO FIND V_{TH}:



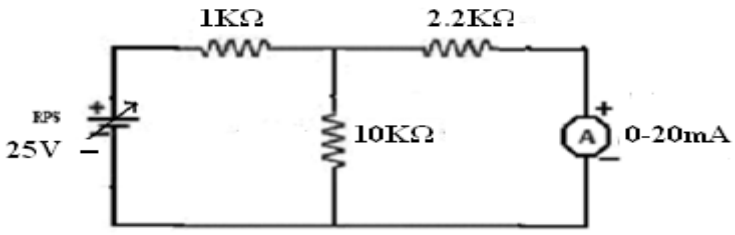
FIG(2)

TO FIND R_{th}:



fig(3)

TO FIND I_N:



Fig(4)

STATEMENTS:

THEVENIN'S THEOREM:

It states that in any lumped, linear network having more number of sources and elements the equivalent circuit across any branch can be replaced by an equivalent circuit consisting of Theremin's equivalent voltage source Vth in series with Theremin's equivalent resistance Rth. Where Vth is the open circuit voltage across(branch) the two terminals and Rth is the resistance seen from the same two terminals by replacing all other sources with internal resistances.

Thevenin's theorem:

The values of VTh and RTh are determined as mentioned in thevenin's theorem. Once the thevenin equivalent circuit is obtained, then current through any load resistance RL connected across AB is given by, $I = \frac{V_T h}{R_{Th}+R_L}$.

Thevenin's theorem is applied to d.c. circuits as stated below.

Any network having terminals A and B can be replaced by a single source of e.m.f. V_{Th} in series with a source resistance R_{Th}

(i) The e.m.f the voltage obtained across the terminals A and B with load, if any removed i.e., it is open circuited voltage between terminals A and B.

(ii) The resistance R_{Th} is the resistance of the network measured between the terminals A and B with load removed and sources of e.m.f replaced by their internal resistances. Ideal voltage sources are replaced with short circuits and ideal current sources are replaced with open circuits.

To find V_{Th}, the load resistor 'RL' is disconnected, then $VTh = \frac{V}{R_1+R_2} X R3$

To find R_{Th},

$$R_{Th} = R2 + \frac{R_1 R_3}{R_1+R_3}$$

Thevenin's theorem is also called as "Helmoltz theorem"

NORTON'S THEOREM:

Norton's theorem states that in a lumped, linear network the equivalent circuit across any branch is replaced with a current source in parallel a resistance. Where the current is the Norton's current which is the short circuit current though that branch and the resistance is the Norton's resistance which is the equivalent resistance across that branch by replacing all the sources sources with their internal resistances.

Nortom's theorem is applied to d.c circuits may be stated as below.

Any linear network having two terminals 'A' and 'B' can be replaced by a current source of current output IN in parallel with a resistance RN.

(i) The output IN of the current source is equal to the current that would flow through AB when A&B are short circuited.

(ii) The resistance RN is the resistance of network measured b/wn A and B with load removed and the sources of e.m.f replaced by their internal resistances.

Ideal voltage source are replaced with short circuits and ideal current sources are replaced with open circuits .

$$I = \frac{V}{R^{I}} = \frac{V(R_2 + R_3)}{R_1R_2 + R_1R_3 + R_2R_3}$$

for short-circuit current,

$$I_N = I \times \frac{R_3}{R_2 + R_3} = \frac{VR_3}{R_1R_2 + R_1R_3 + R_2R_3}$$

PROCEDURE:

1. Connect the circuit as per fig (1)
2. Adjust the output voltage of the regulated power supply to an appropriate value (Say 25V).
3. Note down the response (current, IL) through the branch of interest i.e. AB (ammeter reading).
4. Reduce the output voltage of the regulated power supply to 0V and switch-off the supply.
5. Disconnect the circuit and connect as per the fig (2).
6. Adjust the output voltage of the regulated power supply to 25V.
7. Note down the voltage across the load terminals AB (Voltmeter reading) that gives Vth.
8. Reduce the output voltage of the regulated power supply to 0V and switch-off the supply.
9. Disconnect the circuit and connect as per the fig (3).
10. Adjust the output voltage of the regulated power supply to an appropriate value (Say V =25V).
11. Note down the current (I) supplied by the source (ammeter reading).
12. The ratio of V and I gives the Rth.
13. Reduce the output voltage of the regulated power supply to 0V and switch-off the supply.
14. Disconnect the circuit and connect as per the fig (4).
15. Adjust the output voltage of the regulated power supply to 25V
16. Note down the response (current, I_N) through the branch AB (ammeter reading).
17. Reduce the output voltage of the regulated power supply to 0V and switch-off the supply.
18. Disconnect the circuit.

THERITICAL VALUES:

Tabulation for Thevinen's theorem:

THEORITICAL VALUES	PRACTICAL VALUES
V_{Th}= R_{Th}= I_L=	V_{Th}= R_{Th}= I_L=

Tabulation for Norton's theorem:

THEORITICAL VALUES	PRACTICAL VALUES
I_N= R_N= I_L=	I_N= R_N= I_L=

RESULT:

QUESTIONS:

1) The internal resistance of a source is 2 Ohms and is connected with an external load of 10 Ohms resistance. What is Rth ?
2) In the above question if the voltage is 10 volts and the load is of 50 ohms What is the load current and Vth? Verify IL?
3) If the internal resistance of a source is 5 ohms and is connected with an external load of 25 Ohms resistance. What is Rth?
4) In the above question if the voltage is 20V and the load is of 50 Ohms, What is the load current and IN ? Verify IL ?

PART- B

8. MAGNETIZATION or OPEN CIRCUIT CHARACTERISTICS OF D.C SHUNT GENERATOR

AIM:

To obtain the no load characteristics of a DC shunt generator and to determine the critical field resistance.

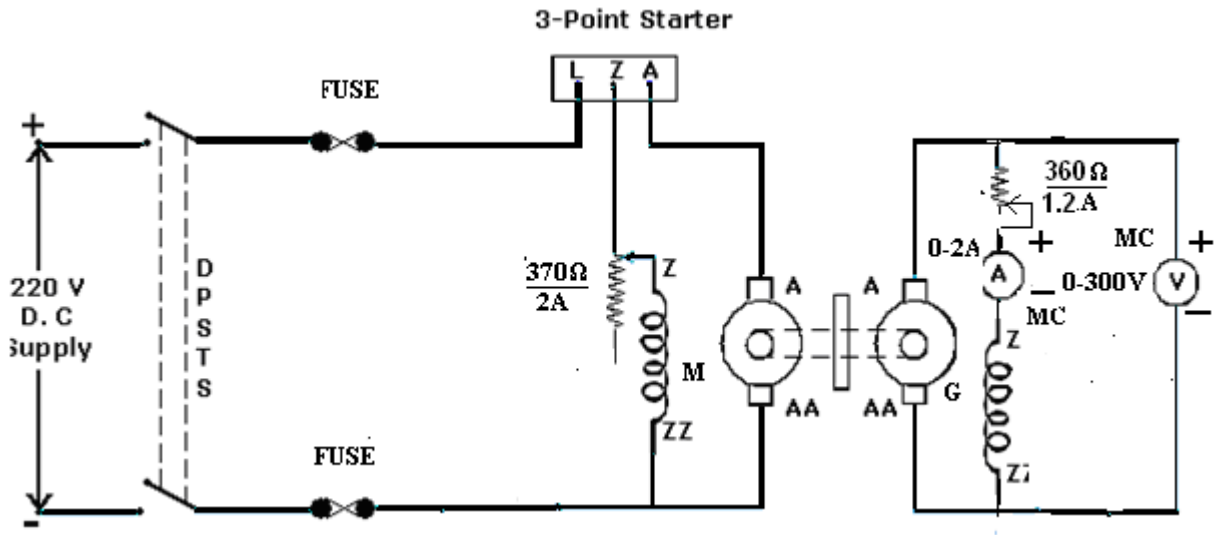
NAME PLATE DETAILS:

S.NO	Characteristics	D.C Motor	D.C Generator
1	Voltage	220V	220V
2	Current	13.6A	20A
3	Speed	1500rpm	1500rpm
4	Power	5HP	3KW

APPARATUS:

S.NO	Name Of The Equipment	Type	Range	Quantity
1	Voltmeters	MC	0-300V	2NO
2	Ammeters	MC	0-2A	1NO
3	Rheostats	WW	370 Ω /2A	2NO
4	Tachometers	Digital	0-10000rpm	1NO

CIRCUIT DIAGRAM:



THEORY:

Magnetization curve is relation between the magnetizing forces and the flux density B. this is also expressed as a relation between the field current and the induced e.m.f , in a D.C machine. Varying the field current and noting corresponding values of induced e.m.f can determine this.
For a self-excited machine the theoretical shape of the magnetization Curve is as shown in the figure. The induced e.m.f corresponding to residual magnetism exists when the field current is zero. Hence the curve starts, a little above the origin on y-axis. The field resistance line R_{sh} is a straight-line passing through the origin.
If field resistance is increased so much that the resistance line does not cut the OCC at all then obviously the machine will fail to exite .If the resistance line just lies along the slope, then machine will just excite. The value of the resistance represented by the tangent to the curve is known as critical field resistance Rc for a given speed.

CRITICAL FIELD RESISTANCE: it is the resistance of the field winding of the generator below which generator fail to build up the voltage.
First OCC is plotted from the the readings then tangent is drawn to its initial position .The slope of this curve gives the critical field resistance.

From the graph the critical field resistance Rc=AB/BC.

PROCEDURE:
1. Connect the circuit as per the circuit diagram shown in fig.
2. Keep the motor field rheostat Rsh at minimum position and generator field rheostat at maximum position.
3. Check that the belt on the pulley is free so that there is no load on the pulley.
4. Switch on the DPST swatch. Start the motor slowly by using starter.
5. Adjust the current so that the motor runs at its rated speed.
6. Now vary the generator field rheostat to increase the field current and take the no load voltage and field current readings.
7. Take the no load voltage values until field gets saturated.
8. Finally set the field rheostats to initial positions then switch off the supply.
9. Draw the graph between generated voltage and field current. Find the critical field resistance from the tangent line.

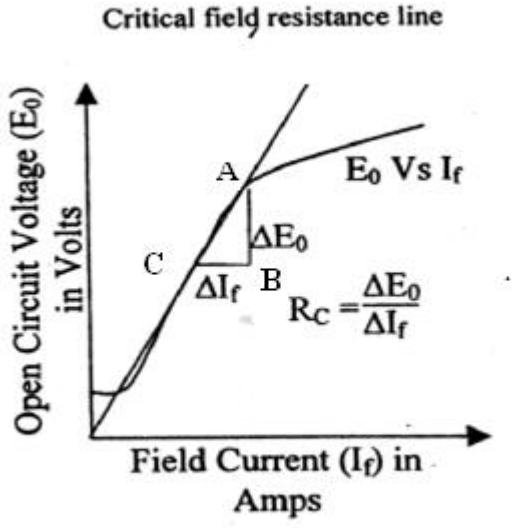
TABULAR COLUMN:

Residual Voltage = Speed=

SNO	I_f(A)	E_g(V)

MODEL GRAPH:

Draw the graph between generated voltage at no load and field current. By taking Generated voltage Eg in volts on Y axis and field current If in amps on X-axis.



PRECAUTIONS:

1) The rheostat is connected such that minimum resistance is included in field circuit of motor.
2) The rheostat is connected such that maximum resistance is included in field circuit of generator.
3) Starter handle is moved slowly.

RESULT:

QUESTIONS:

1. What is meant by critical field resistance?
2. Residual magnetism is necessary for self excited generators or not.
3. Why this test is conducted at constant speed?

9. SWINBURNE'S TEST ON D.C SHUNT MACHINE

AIM: To perform Swinburne's test on the given D.C machine and predetermine the efficiency at any desired load both as motor and as generator.

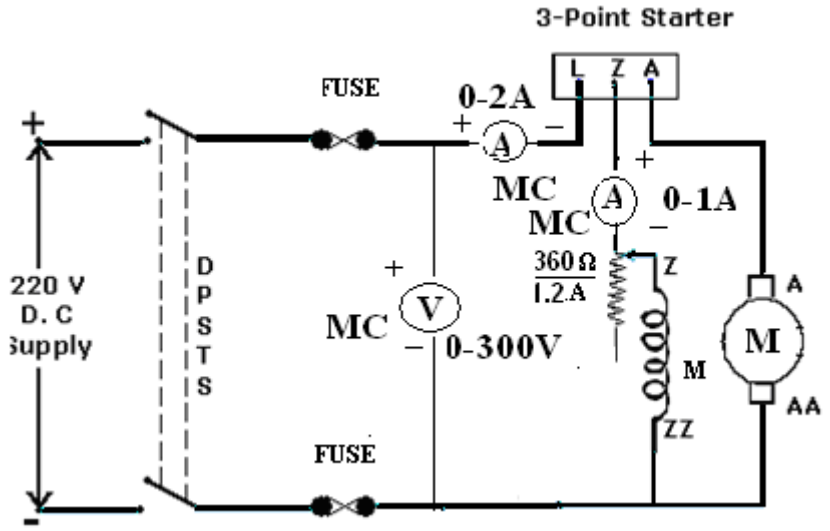
NAME PLATE DETAILS:

S.NO	Characteristic	D.C Motor
1	Voltage	220V
2	Current	20A
3	Speed	1500rpm
4	Power	5HP

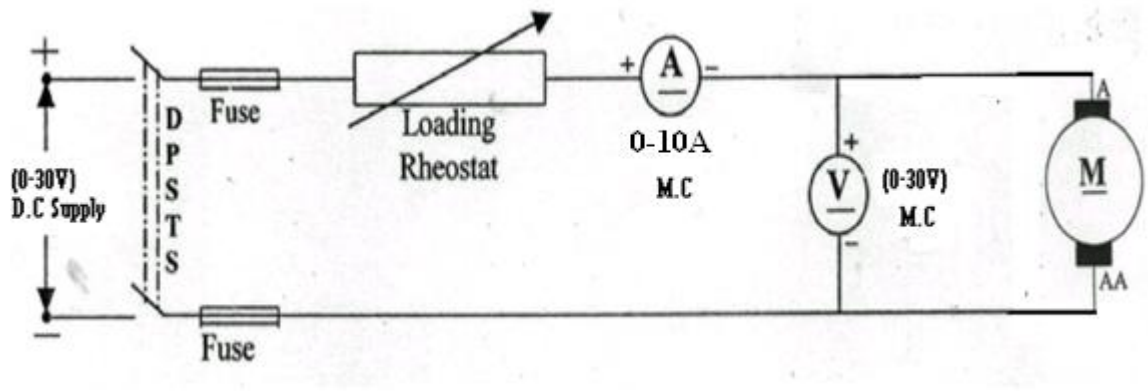
APPARATUS REQUIRED:

S.NO	Name Of The Equipment	Type	Range	Quantity
1	Ammeter	MC	0-2A,0-1A,0-10A	3NO
2	Voltmeter	MC	0-30V,0-300V	2NO
3	Rheostat	WW	370 Ω /2A	1NO
4	Tachometer	Digital	1000rpm	1NO

CIRCUIT DIAGRAM:



CIRCUIT DIAGRAM TO FIND ARMATURE RESISTANCE:



THEORY:

This test is to find out the efficiency of the machine .It is a simple indirect method in which losses are determined separately and from their knowledge, efficiency at any desired load can be predetermined. The only test needed is no-load test. This test cannot be performed on DC series motor. The machine is run as a no load shunt motor at rated speed and with a rated terminal voltage .However, this test is applicable to those machines in which flux is practically constant.

The constant losses in a dc shunt machine= Wc = stray losses (magnetic & mechanical losses) +shunt field copper losses.

$$Wc = \text{No load input} - \text{No load armature copper losses}$$
$$= VI_{L0} - I^2_{ao}Ra \text{ where Ra is the armature resistance}$$
$$\text{And } I_{ao}=I_L-I_{sh}$$

PROCEDURE

1) Make all the connections are as per the circuit diagram.
2) Keep the field rheostat in **minimum** resistance position.
3) Excite the motor with **220V, DC** supply by closing the **DPST** switch and start the Motor by moving the handle of 3-point starter from **OFF** to **ON** position.
4) By adjusting the rheostat in motor field bring the speed of the motor to its rated value. Note down the readings of Ammeter and Voltmeter at no load condition.
5) The necessary calculations to find efficiency of machine as motor & generator at any given value of armature current is done.

TO FIND ARMATURE RESISTANCE (Ra):

1) Connect the circuit per the circuit diagram
2) Keep the rheostat in maximum position.
3) Now excite the motor terminals by 30V supply by closing DPST switch.
4) Note down the readings of Ammeter and voltmeter.

MODEL CALCULATIONS:-

For motor:

$I_L= I_a+I_f$

No load losses = $W_o = VI_o - I^2_{ao}Ra$

Input = VI

Cu losses = $I_a^2R_a$

Total losses =No load losses + cu losses
Output = Input-Total losses
%Efficiency (η) = (Output / Input)*100

For generator:
$I_a = I_L + I_f$
No load losses = $W_o = V I_o - I^2_{ao}Ra$
Output = VI
Cu losses = Ia^2 Ra
Total losses =No load losses + cu losses
Input =Output+ Total losses
%Efficiency (η) = (Output / Input)*100

TABULAR COLOUMN:

S.NO	Voltmeter reading V in Volts	Ammeter Reading I in Amps	Ammeter reading I_{sh} in Amps	Speed in RPM

ARMATURE RESISTANCE (Ra):

S.No	Voltage	Current

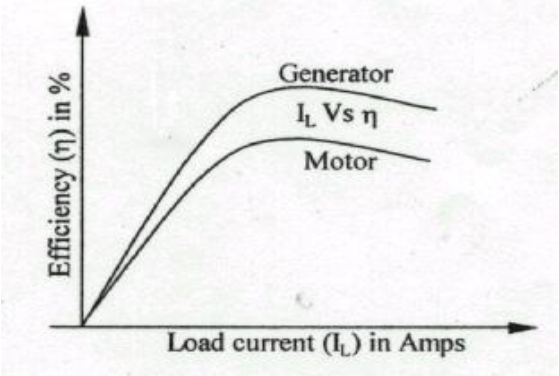
CALCULATION TABLE:
As a Motor:

S.NO	I_L (A)	$I_a=(I_L-I_{sh})$ in A	$W=I_a^2R_a$ in watts	Total losses	%Efficiency

As a Generator:

S.NO	I_L (A)	$I_a=(I_L+I_{sh})$ in A	$W=I_a^2R_a$ in watts	Total losses	%Efficiency

MODEL GRAPH:



PRECAUTIONS:

1. We should start the motor under no load
2. Take the reading without parallax error.
3. The connections must be tight.
4. If voltmeter gives ding then interchange voltmeter terminal connecting of voltmeter.

RESULT:

QUESTIONS:

1. Why the magnetic losses calculated by this method are less than the actual value?
2. Is it applied to D.C series machines?
3. Comment on the efficiency determined by this method.

10. BRAKE TEST ON D.C SHUNT MOTOR

AIM:

To conduct the brake test on a D.C shunt motor and to draw its performance curves.

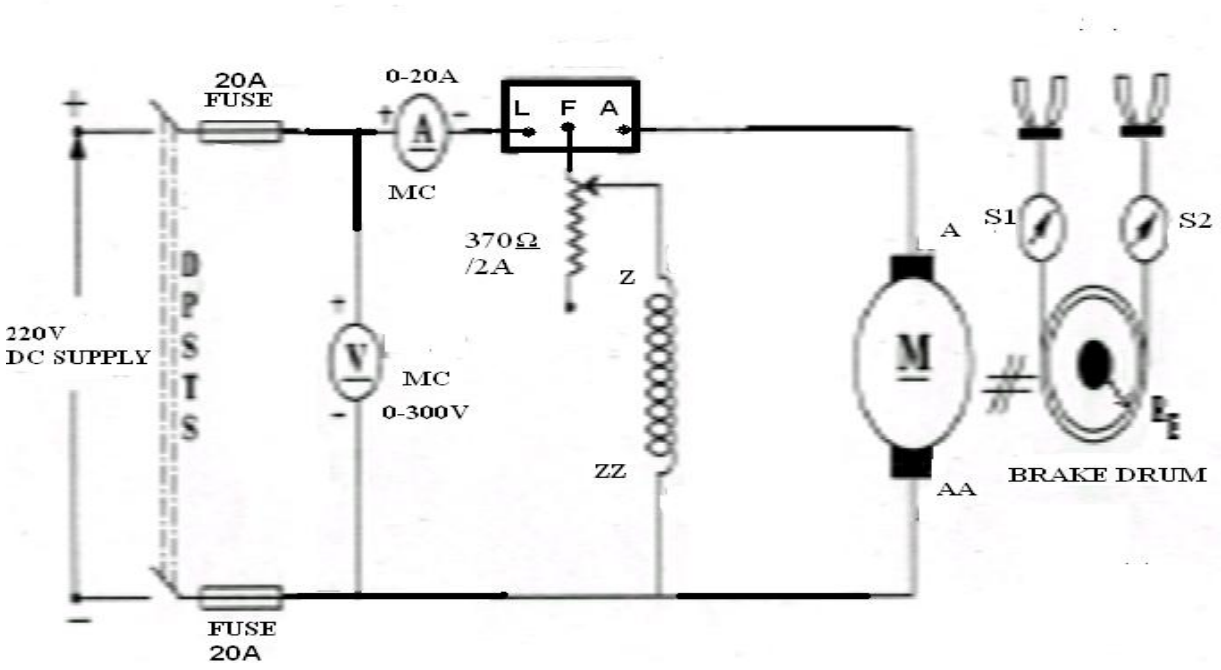
NAME PLATE DETAILS:

S.NO	Characteristic	D.C Motor
1	Voltage	220V
2	Current	20A
3	Speed	1500rpm
4	Power	5HP

APPARATUS REQUIRED:

S.NO	Description	Type	Range	Quantity
1	Ammeter	MC	0-20A	1NO
2	Voltmeter	MC	0-300V	1NO
3	Rheostat	WW	370 Ω /2A	1NO
4	Tachometer	Digital	0-10000rpm	1NO

CIRCUIT DIAGRAM:



THEORY:

This test is direct test to find the efficiency of the DC shunt motor. In this test the motor directly loaded by connecting brakes which are with pulley and motor is subjected to rated load and entire power is wasted. belt around the water cooled pulley has its ends attached to spring balances s1and s2.The belt tightening hand wheels h1 and h2 help in adjusting the load on the pulley so that the load on the motor can be varied.

Output power of the motor = (S1-S2)*Re*9.81*w (watts)
S1, S2 = weights on the pulley.
Re= Effective radius of the pulley.
w=motor speed in rad/sec.
If V is the terminal voltage IL is the line current
Power in put =$V*I_L$ watts.
Efficiency (%η)=$(w(S1-S2)*Re*9.81/V*I_L)*100$

PROCEDURE:

1. All the connections are as per the circuit diagram.
2. **220V**, DC supply is given to the motor by closing **DPST** switch.
3. Move the 3-point starter handle form **'OFF'** to **'ON'** position slowly and motor starts running.
4. Vary the field rheostat until the motor reaches its rated Speed and take voltmeter and ammeter readings.
5. Apply the land by break drum pulley and for each applications of load the Corresponding Voltmeter (V), Ammeter (I), spring forces S1 & S2 and Speed (N) Readings are noted.
6. Calculate output & efficiency for each reading.
7. Note down all the readings in the tabular form carefully.
8. Remove the load slowly and keep the rheostat as starting position and switch **'OFF'** the supply by using **DPST** switch.

TABULAR COLUMN:

S. NO	Voltage (V)	Current (A)	Input =VI watts	Forces in KG S_1	S_2	Net force F = S1~S2 in kg	Torque(T) =F*Re*9.81 (N-M)	Speed in RPM (N)	O/p= 2πNT/60 (Watts)	%Efficiency η=output/input

GRAPH:

The graph is drawn between

a) Output in Watts Vs Speed(N) in RPM

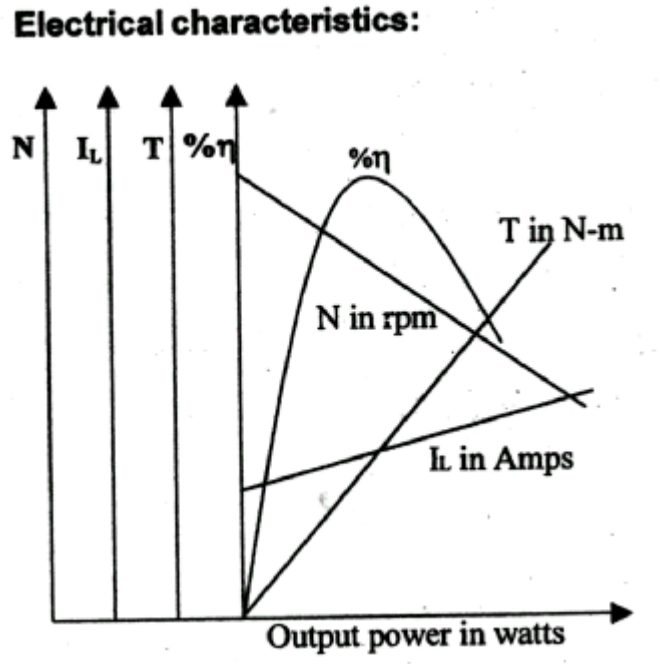
b) Output in Watts Vs Torque (T) in N-m

c) Output in Watts Vs Current (I) in A

d) Output in Watts Vs Efficiency (%η)

By taking output in Watts on X axis and speed, Torque, current, Efficiency onY- axis .

MODEL GRAPH:



PRECAUTIONS:

1. Initially 3-point starter should be kept at 'OFF' position and later it must be varied slowly and uniformly from 'OFF' to 'ON' position.
2. The field regulator must be kept at its minimum output position.
3. The brake drum of the motor should filled with cold water.
4. The motor should be started without load.

RESULT:

QUESTIONS:

1 .Why a 3-point starter is used for starting a D.C shunt motor?

2. If a 3-point starter is not available, how can a D.C motor be started?

3. Explain the function of overload release coil in 3-point starter.

11. OC & SC TESTS ON 1 – PHASE TRANSFORMER

AIM:

To conduct Open circuit and Short circuit tests on 1-phase transformer to pre-determine the efficiency, regulation and equivalent parameters.

NAME PLATE DETAILS:

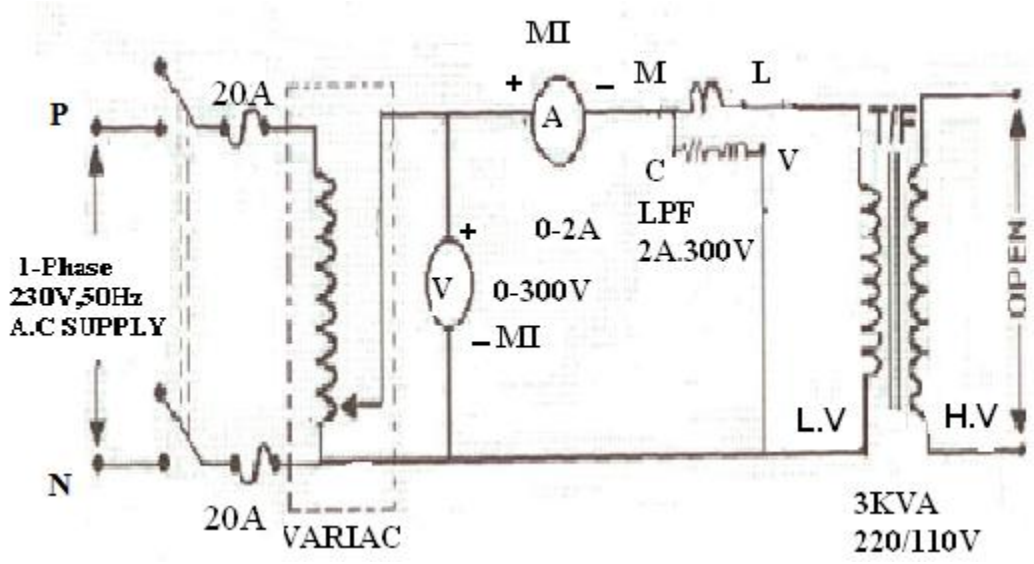
Voltage Ratio	220/110V
Full load Current	13.6A
KVA RATING	3KVA

APPARATUS:

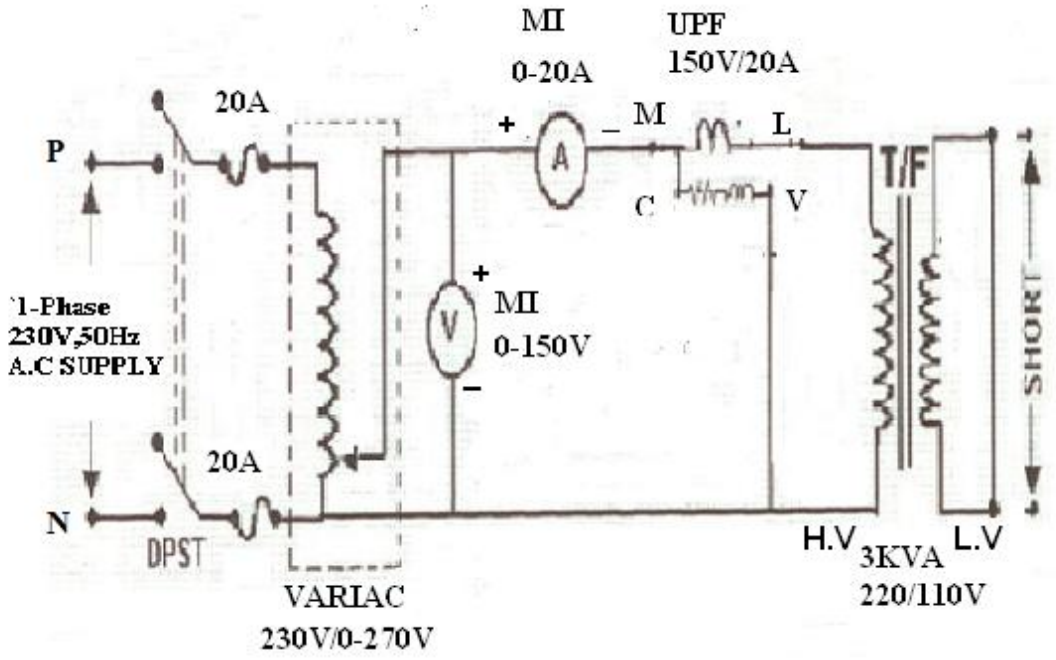
S.NO	Description	Type	Range	Quantity
1	Ammeter	MI	0-20A 0-5A	2NO
2	Voltmeter	MI	0-150V 0-300V	2NO
3	Wattmeter	LPF UPF	2A,!50V 20A,300V	2NO
4	Auto transformer	-	230/0-270V	1NO
5	Transformer	-	220V/110V	1NO

CIRCUIT DIAGRAM:

OPEN CIRCUIT TEST:



SHORT CIRCUIT TEST:



THEORY:

Transformer is a device which transforms the energy from one circuit to other circuit without change of frequency.

The performance of any transformer calculated by conducting tests .OC and SC tests are conducted on transformer to find the efficiency and regulation of the transformer at any desired power factor.

OC TEST:

The objectives of OC test are

1. To find out the constant losses or iron losses of the transformer.
2. To find out the no load equivalent parameters.

SC TEST:

The objectives of OC test are

1. To find out the variable losses or copper losses of the transformer.
2. To find out the short circuit equivalent parameters.

By calculating the losses and equivalent parameters from the above tests the efficiency and regulation can be calculated at any desired power factor.

PROCEDURE (OC TEST):

1. Connections are made as per the circuit diagram
2. Initially variac should be kept in its minimum position
3. Close the DPST switch.
4. By varying Auto transformer bring the voltage to rated voltage
5. When the voltage in the voltmeter is equal to the rated voltage of HV winding note down all the readings of the meters.
6. After taking all the readings bring the variac to its minimum position
7. Now switch off the supply by opening the DPST switch.

PROCEDURE (SC TEST):

1. Connections are made as per the circuit diagram.
2. Short the LV side and connect the meters on HV side.
3. Before taking the single phase, 230 V, 50 Hz supply the variac should be in minimum position.
4. Now close the DPST switch so that the supply is given to the transformer.
5. By varying the variac when the ammeter shows the rated current
(i.e. 13. 6A) then note down all the readings.
6. Bring the variac to minimum position after taking the readings and switch off the supply.

O.C TEST OBSERVATIONS:

S.NO	V_0(VOLTS)	I_0(AMPS)	W_0(watts)

S.C TEST OBSERVATIONS:

S.NO	V_{SC}(VOLTS)	I_{SC}(AMPS)	W_{SC}(watts)

CALCULATIONS:

(a)Calculation of Equivalent circuit parameters:
Let the transformer be the step down transformer.

(i) Parameters calculation from OC test

$\cos \phi_0 = \frac{W_o}{V_o I_o} =$

$I_w = I_0 \cos \phi_0 =$

$R_0 = \frac{V_1}{I_w} =$

$I_\mu = I_0 \sin \phi_0 =$

$X_0 = \frac{V_1}{I_\mu} =$

$K = \frac{V_2}{V_1} =$

(ii) Parameters calculation from SC test

$R_{01} = \frac{W_{SC}}{I_{sc}^2} =$

$X_{01} = \sqrt{Z_{01}^2 - R_{01}^2} =$

$Z_{01} = \frac{V_{SC}}{I_{SC}} =$

(b) Calculations to find efficiency:

For 'n ' fraction of full load

Cupper losses = $n^2 \times W_{sc}$ watts

where W_{sc} = full load copper losses

Constant losses = W_0 watts

Output = n x KVA x cos ϕ [cos ϕ may be assumed

Input = output + Cu. Loss + constant loss

% $efficiency = \frac{Output}{Input} \times 100$ **=**

(C)Calculation of Regulation at full load:

$$\% \text{ Regulation} = \frac{I_1 R_{01} \cos\phi \pm I_1 X_{01} \sin\phi}{V_1} \times 100 =$$

'+' for lagging power factors

'–' for leading power factors

TBULAR COLUMN:

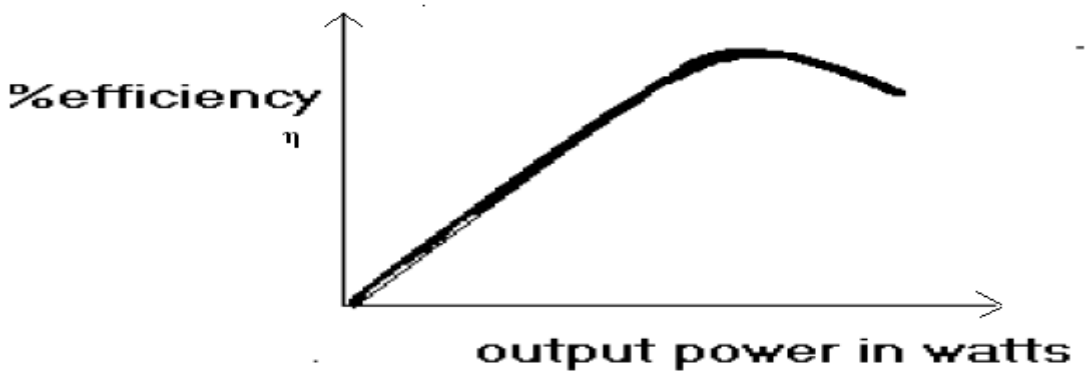
S.NO	% OF LOAD	EFFICIENCY

TABULATION:

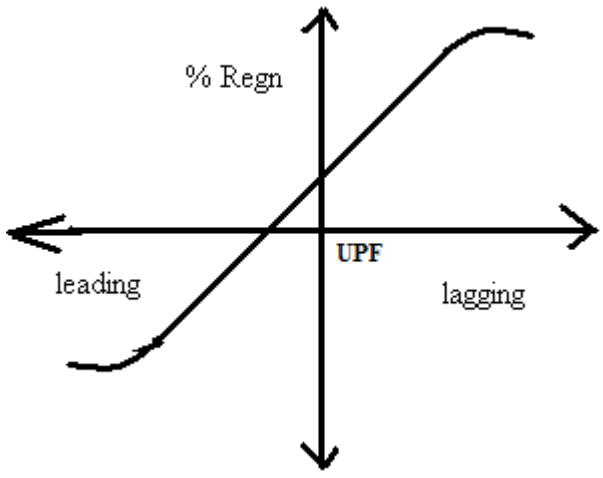
LAGGING POWER FACTOR			LEADING POWER FACTOR		
SNO	PF	%REG	SNO	PF	%REG
1	0.2			0.2	
2	0.4			0.4	
3	0.6			0.6	
4	0.8			0.8	
5	UNITY			UNITY	

MODEL GRAPHS:

1. EFFICIENCY VS OUTPUT



2. REGULATION VS POWER FACTOR



RESULT:

QUESTIONS:

1) What is a transformer?
2) Draw the equivalent circuit of transformer?
3) What is the efficiency and regulation of transformer?

12. LOAD TEST ON 1-PHASE TRANSFORMER

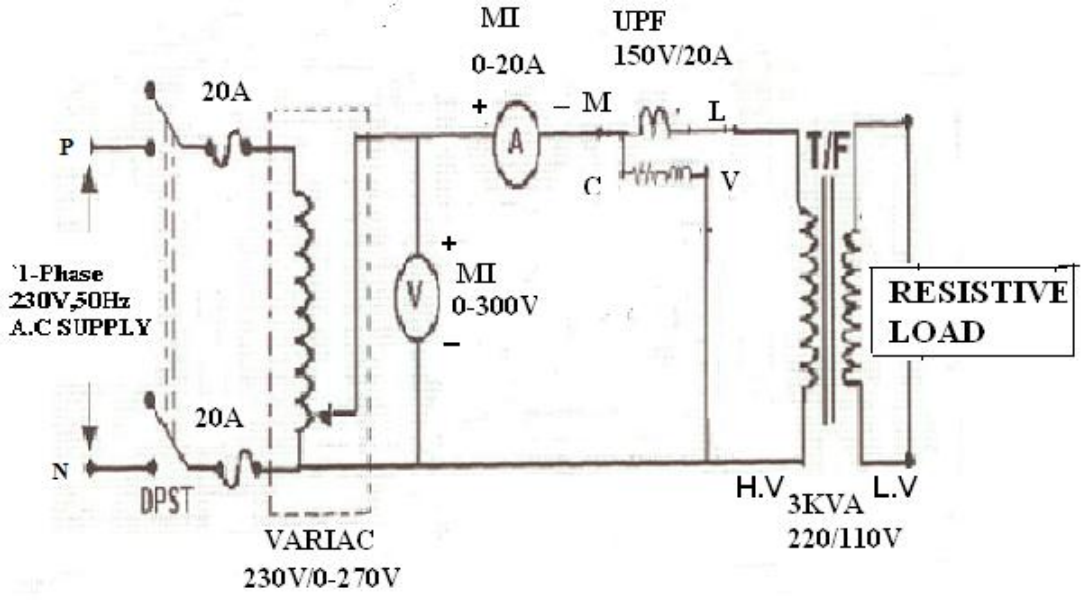
AIM: To find out efficiency by conducting the load test on 1-ϕ Transformer.

APPARATUS REQUIRED:

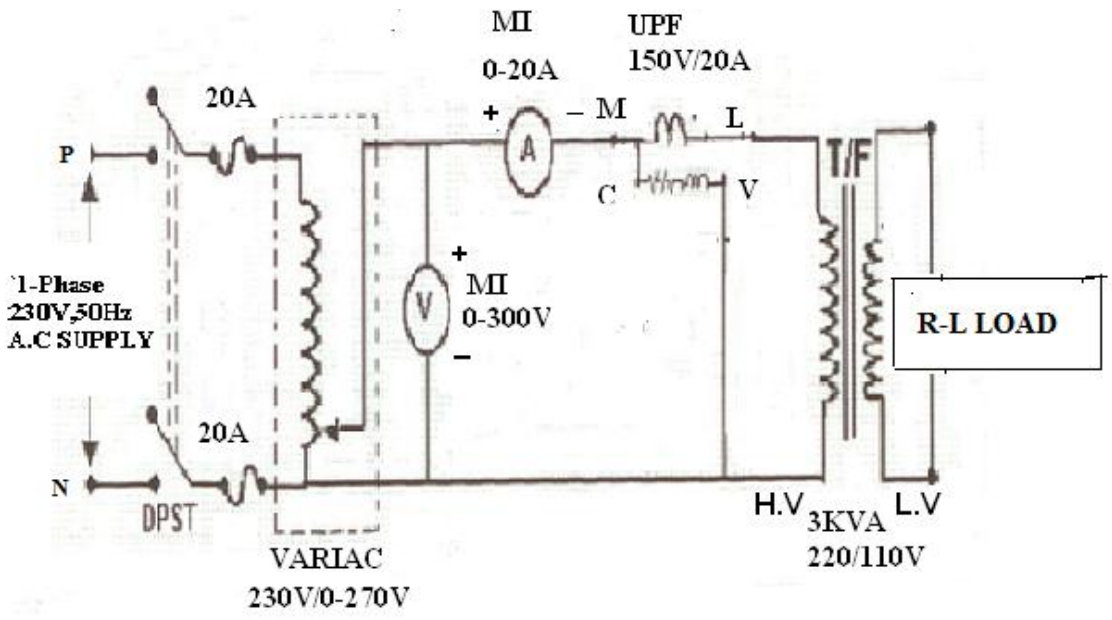
S.NO	APPARATUS	TYPE	RANGE	QUANTITY
1	1-ϕ AUTO Transformer	VARIABLE VOLTAGE	0-270V	01
2	1-ϕ Transformer	Shell type	220/110V	01
3	Voltmeter	MI	0-300V	01
4	Ammeter	MI	0-20A	01
5	Resistive load	Rheostat & variable	0-20A	01
6	Wattmeter	UPF	300V/20A	01
7	Connecting wires			Required number

CIRCUIT DIAGRAM:

RESISTIVE LOAD



R-L LOAD



PROCEDURE:

1) Connect the circuit as shown in above fig.
2) Switch on the input AC supply.
3) Slowly vary the auto transformer knob up to rated input voltage of main transformer.
4) Apply the load slowly up to rated current of the transformer.
5) Take down the voltmeter and ammeter readings.
6) Draw the graph between efficiency and output power.

TABULAR COLUMN (RESISTIVE LOAD):

S.NO	Load Current (amps)	Voltage (volts)

TABULAR COLUMN(R-L LOAD)

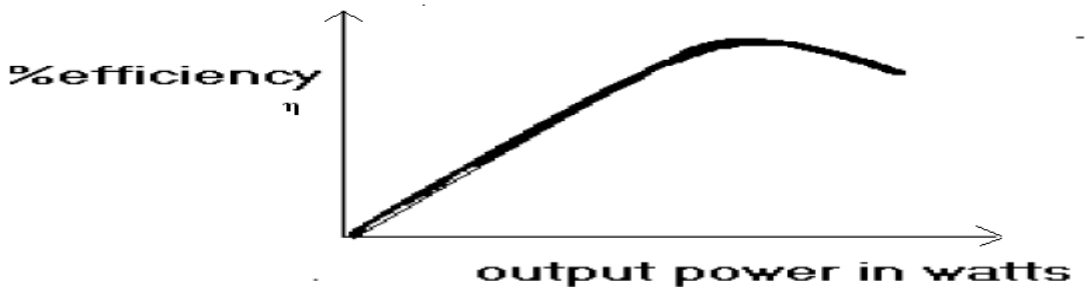
S.NO	Load Current (amps)	Voltage (volts)

OBSERVATION TBLE:

S.NO	% OF LOAD	EFFICIENCY

MODEL GRAPHS:

EFFICIENCY VS OUTPUT



RESULT:

QUESTIONS:

1) What is load test on transformer and what is the advantage of this test?
2) What is other test to determine the efficiency and regulation of transformer?